

# **THALES Microelectronics S.A.**

## **FAILURE ANALYSIS LABORATORY**

# **THERMAL LASER STIMULATION**

## **(TLS / OBIRCH / TIVA)**

# TLS in the FA flow

***I.C. FA flow***

Electrical  
diagnostic

*Defect  
localization*

Physical  
analysis

## Current related defects

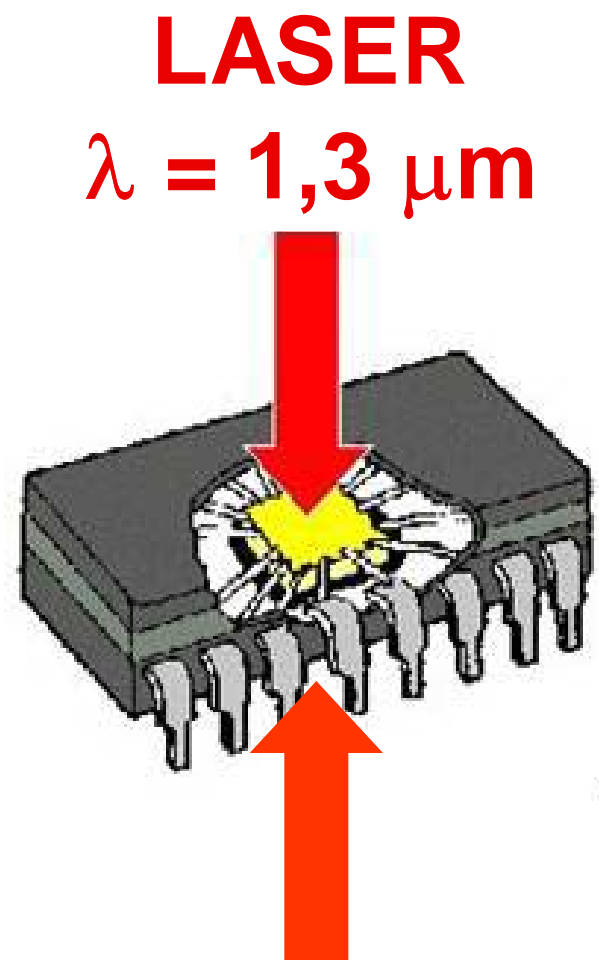
Emission  
microscopy

Thermal Laser  
Stimulation

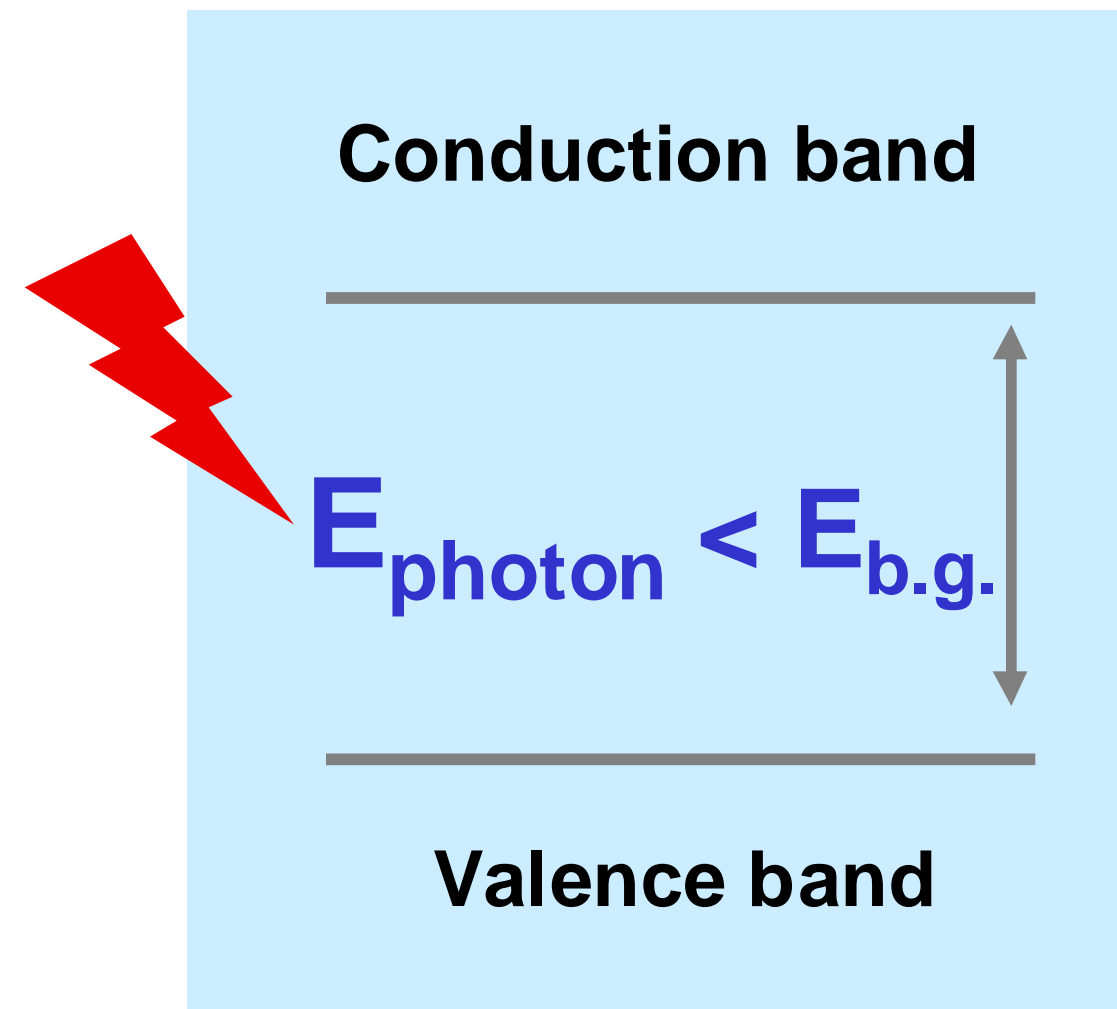
–  $I_{leakage}$  junctions  
–  $I_{leakage}$  oxides

–  $I_{leakage}$  metallic  
shorts

# TLS Principles



- Heating
- No e-h pair generation



**High absorption in:**

- Metals
- Polysilicon
- Highly doped silicon

$$\alpha_{\text{Aluminium}} = 1,1 \times 10^6 \text{ cm}^{-1}$$

# Laser Heating of Metals

**Electric current density :**

$$\mathbf{j} \cong \sigma [\mathbf{E} + Q(-\nabla T)]$$

$\uparrow T^\circ \rightarrow$  **Current variation**

$\nabla T^\circ \rightarrow$  **Additional current**

# A. Resistance Variation

$$\Delta R = \frac{\rho_0 L}{S} (\alpha_{TCR} - 2\delta_T) \Delta T$$

$\alpha_{TCR}$  → Temperature  
Coefficient of Resistivity

$\delta_T$  → Coefficient of  
Thermal linear dilatation

## Aluminium

$$\alpha_{TCR} = 4,29 \times 10^{-3}$$

$$\delta_T = 2,36 \times 10^{-5}$$

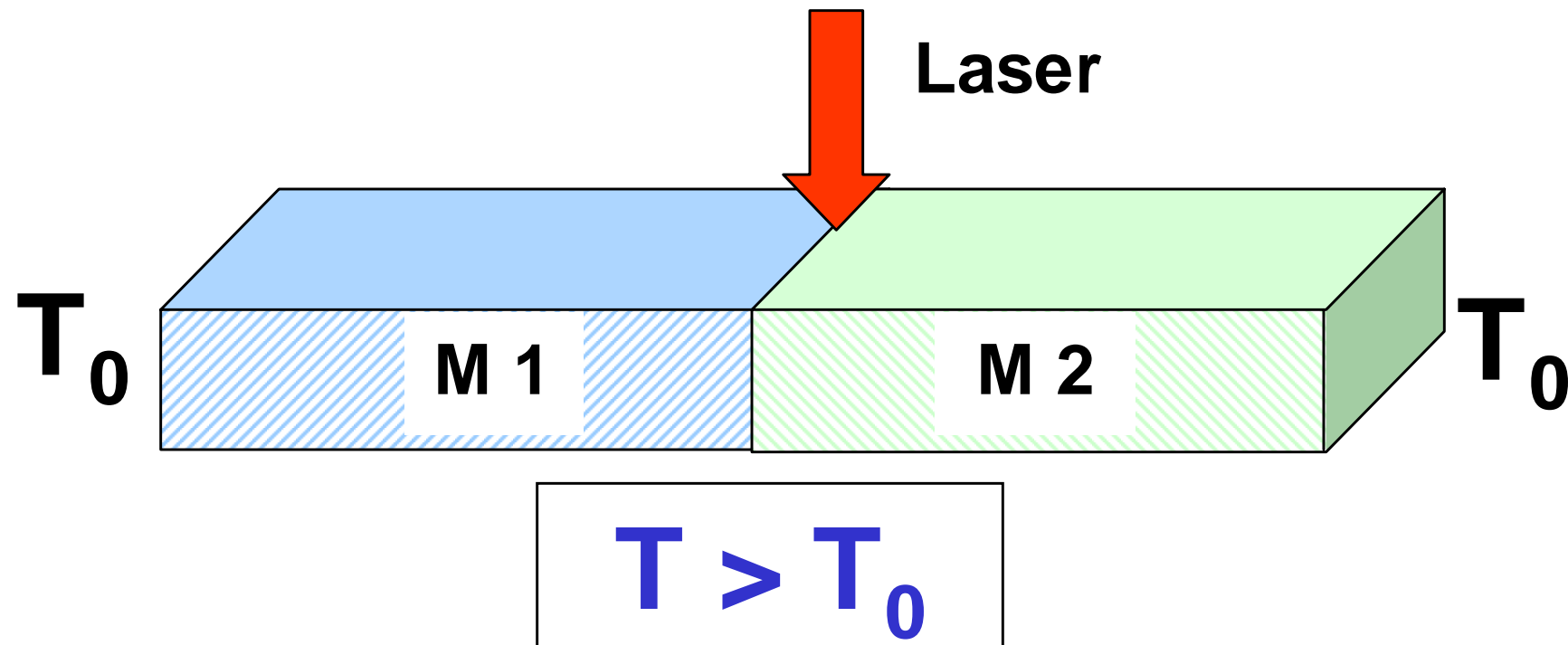
## Current Source (TIVA)

$$\Delta V = \Delta R \cdot I$$

## Voltage Source (OBIRCH)

$$\Delta I = -\left(\Delta R / R^2\right) V$$

## B. Electromotive Force Generation



$$V_{12} = (Q_1 - Q_2)(T - T_0) = Q_{12}(T - T_0)$$

$Q \rightarrow$  Thermoelectric power or Seebeck coefficient

$Q_{12} \rightarrow$  Relative Thermoelectric power

Materials	$Q_{12}$ ( $\mu\text{V}/^\circ\text{C}$ )
Al / W	7,0
Al / n+ Poly	-121
Al / n+ Si ( $10^{20}\text{cm}^{-3}$ )	-105

# TLS Model

## Parameters:

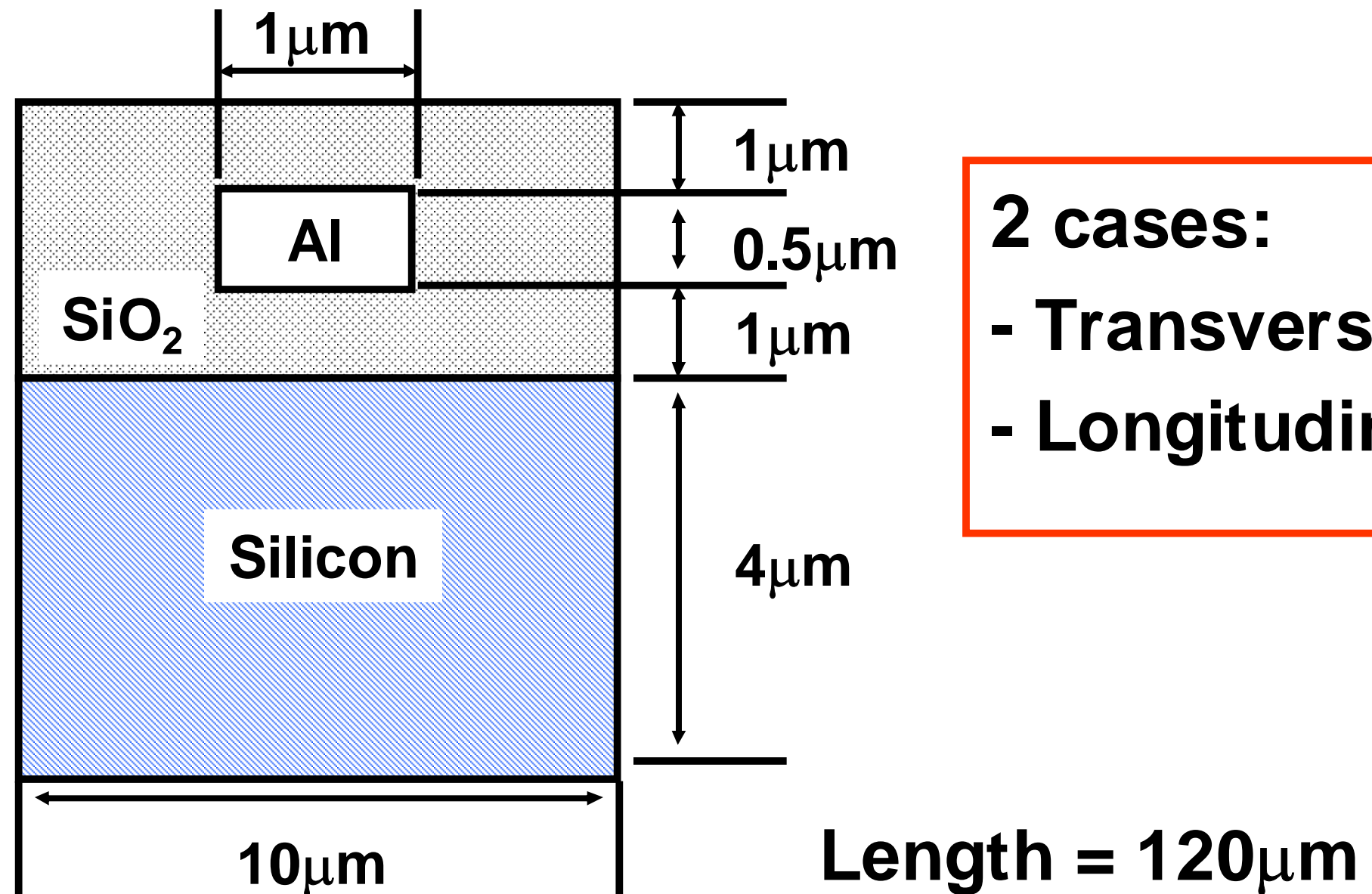
$T_{ini}$ : 25°C

$P_{laser}$ : 100mW

$R_{laser}$ : 0,65μm

$V_{fast}$ : 1,23m/s

$V_{slow}$ : 0,00768m/s

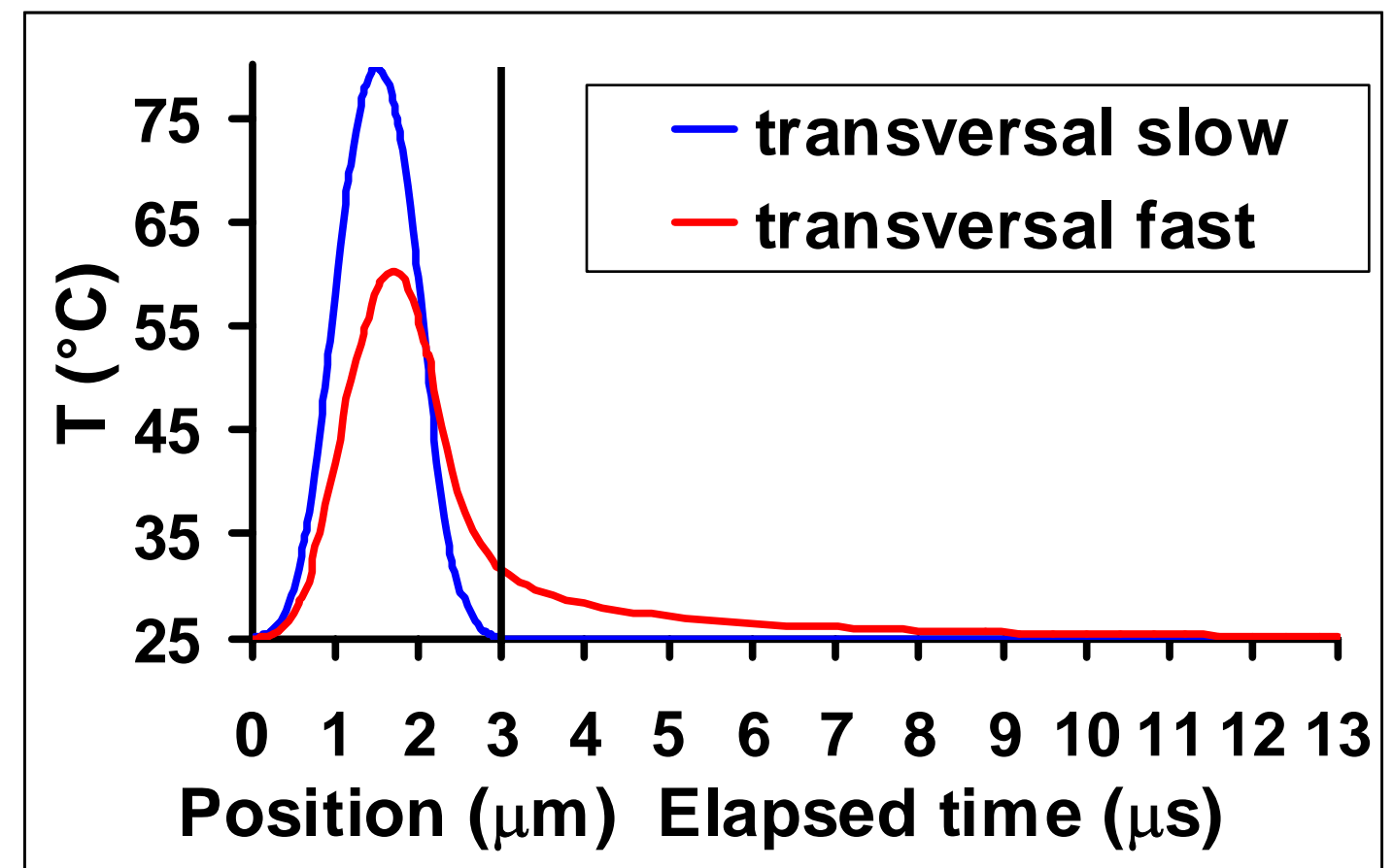
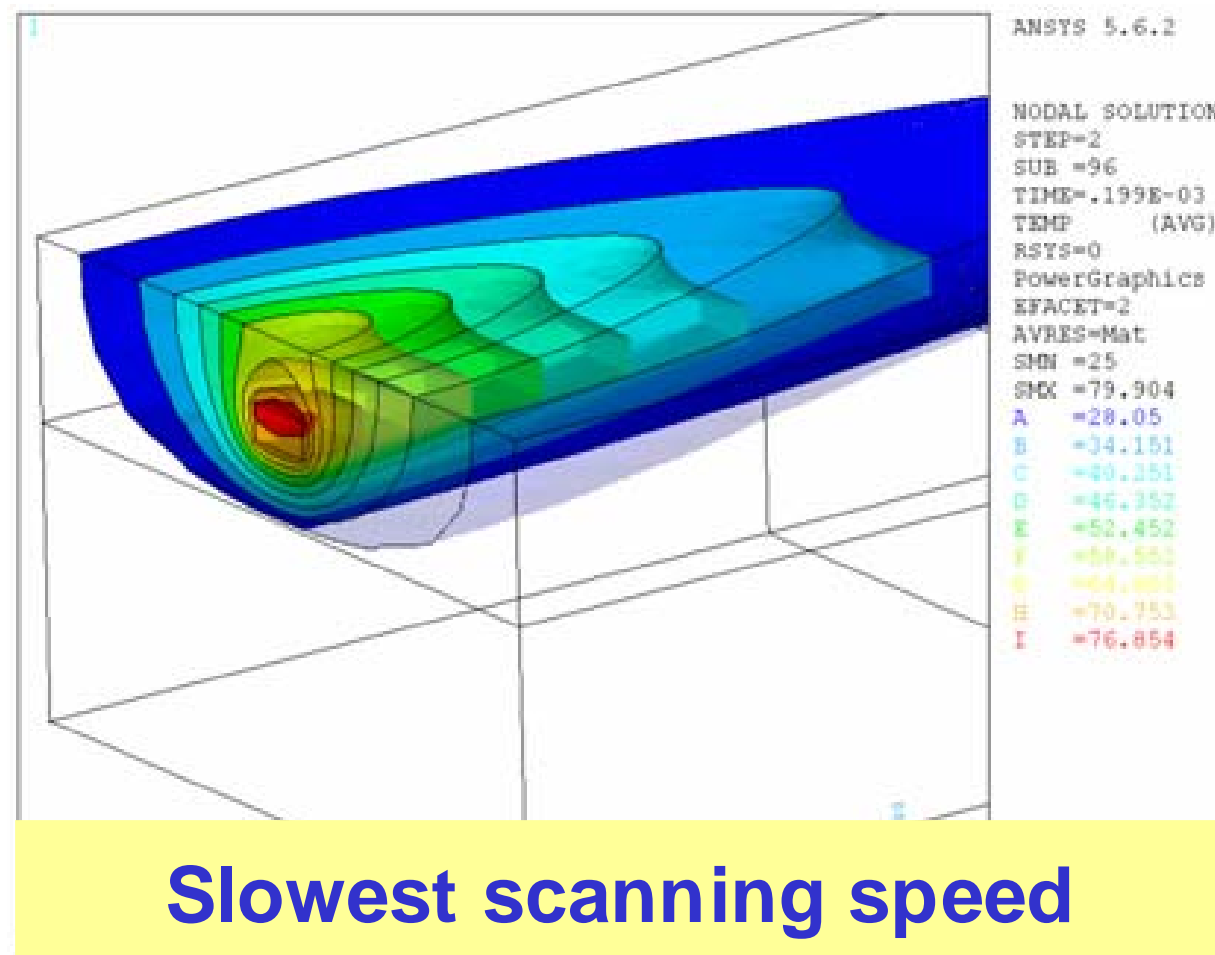


**2 cases:**  
 - Transversal  
 - Longitudinal

**Model: 1μm Al line, Gaussien Laser**

# A. Transversal Case

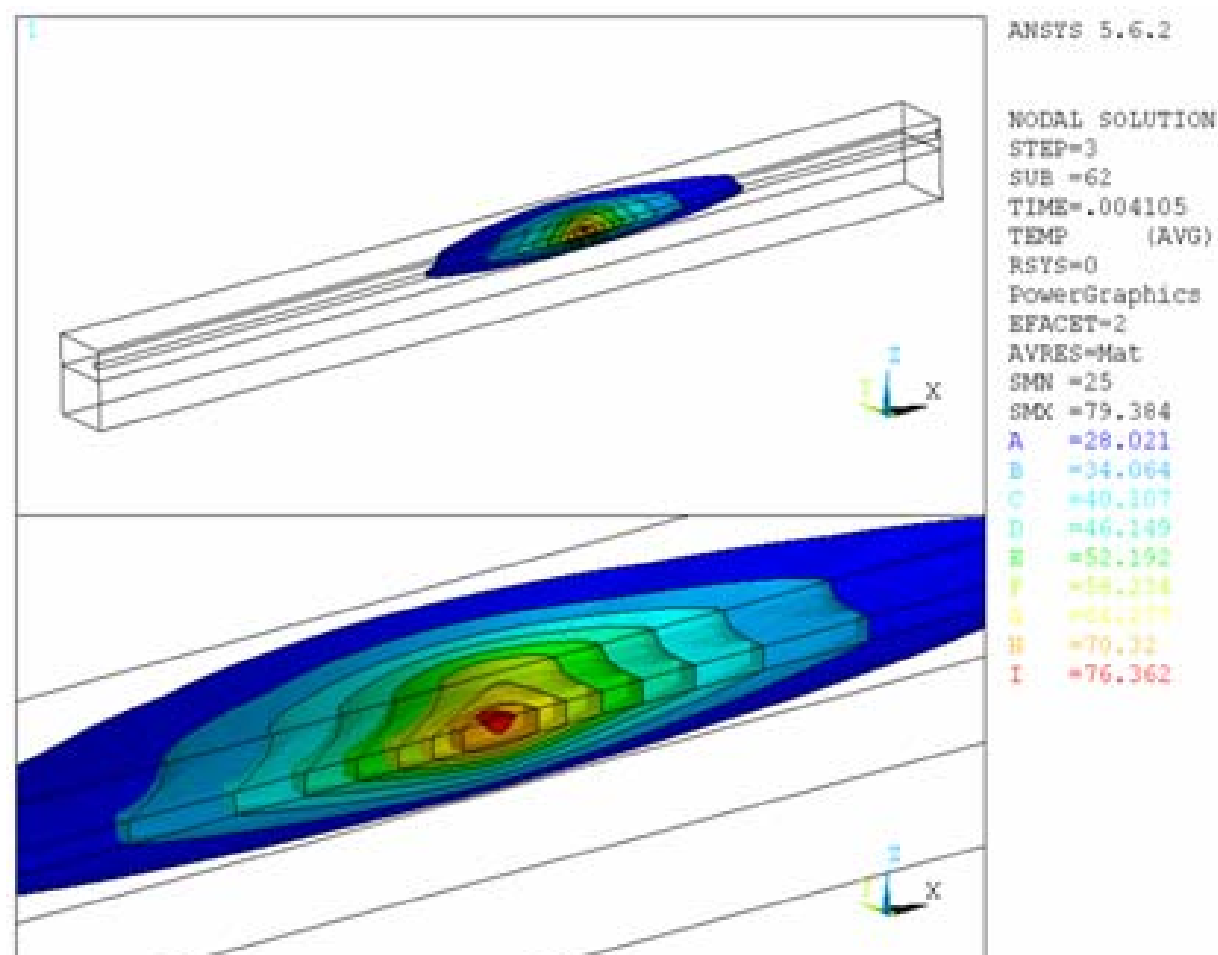
- Rapid thermal equilibrium and heat dissipation
- Hottest temperature occurs at laser spot



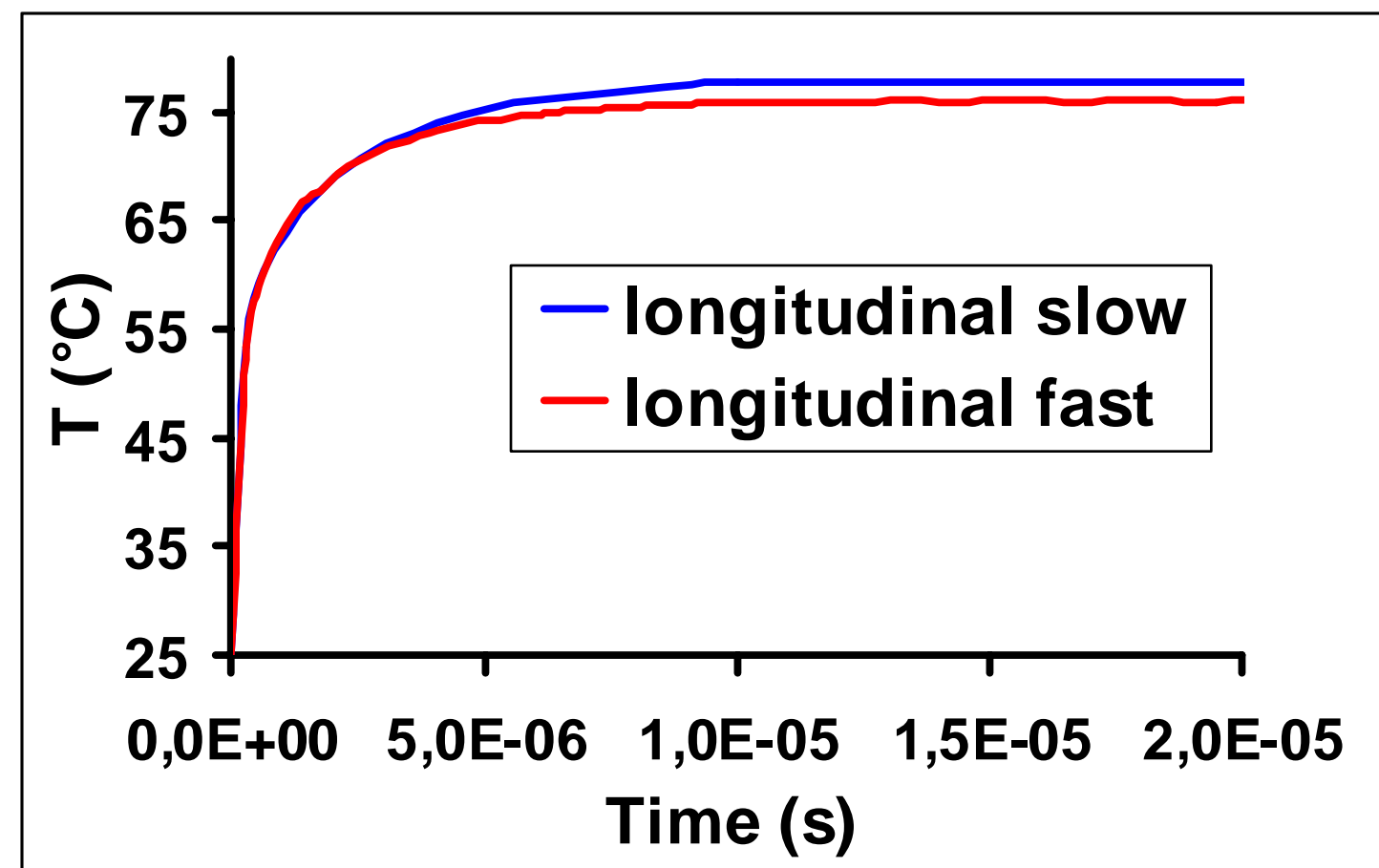


## B. Longitudinal Case

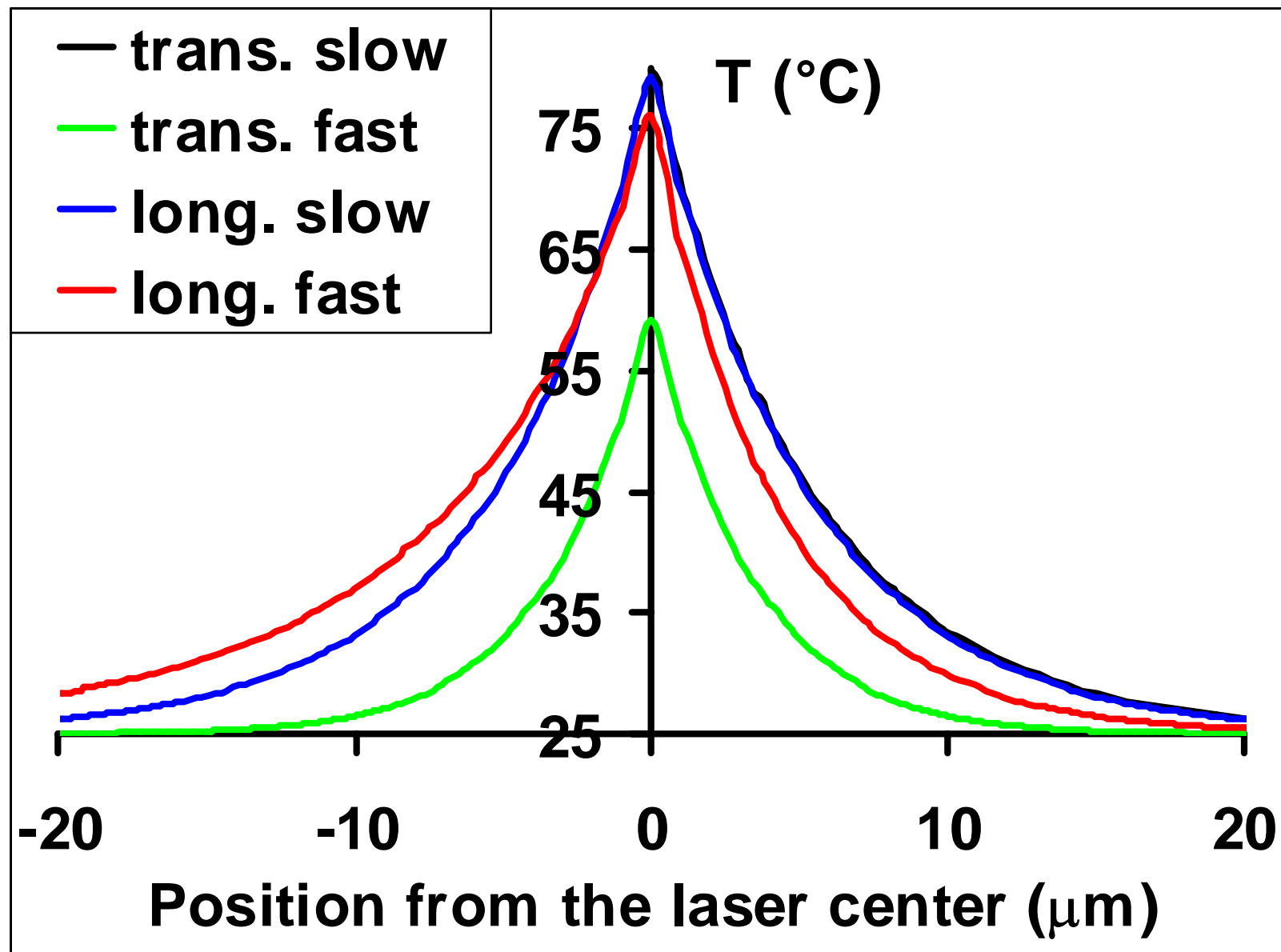
- Thermal equilibrium reached after  $10\mu\text{s}$



Slowest scanning speed



# Temperature Calculation



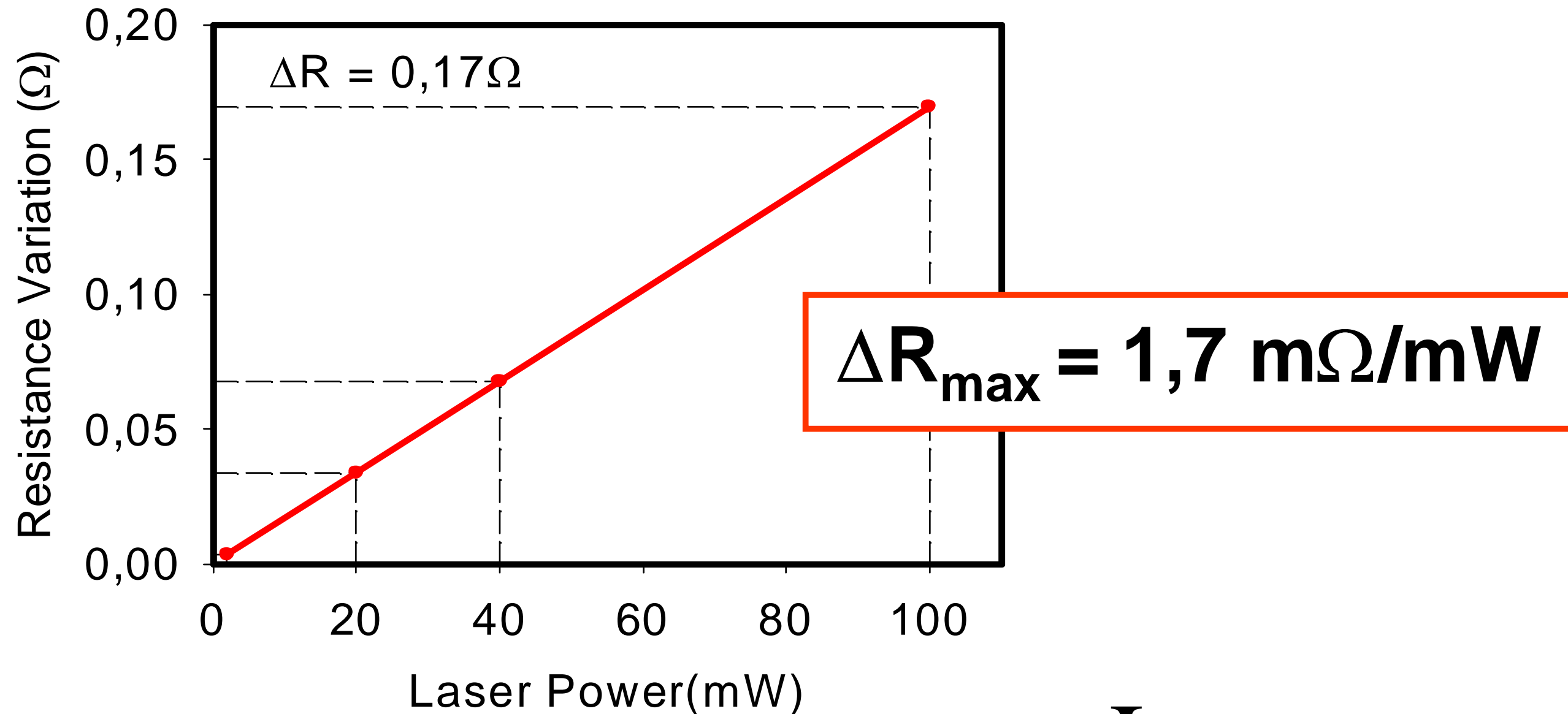
**At thermal equilibrium:**

**Thermal spreading limited to  $\sim 30\mu\text{m}$**

**Temperature varies linearly with laser power**

$$\Delta T_{\text{max}} = 0.55^{\circ}\text{C}/\text{mW}$$

# Resistance Calculation



$$\Delta R = \frac{\rho_0 \alpha_{\text{TCR}} L}{S} (T_{\text{Moy}} - T_0)$$

# Model Conclusion

Localization of defects and lines submitted to  $I_{\text{leakage}}$

$\Delta R \propto 1/\infty$  Section

$\Delta V \propto I_{\text{leakage}}$

Localization of junctions and interface defects

$Q_{12}$  or  $\Delta T$

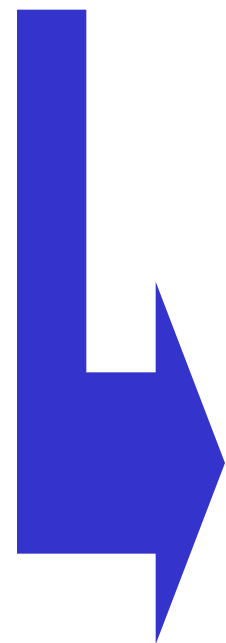
Precise localization

Thermal diffusion  $< 30\mu\text{m}$

$T_{\text{max}}$  at center of line and laser beam

# TLS System Requirements

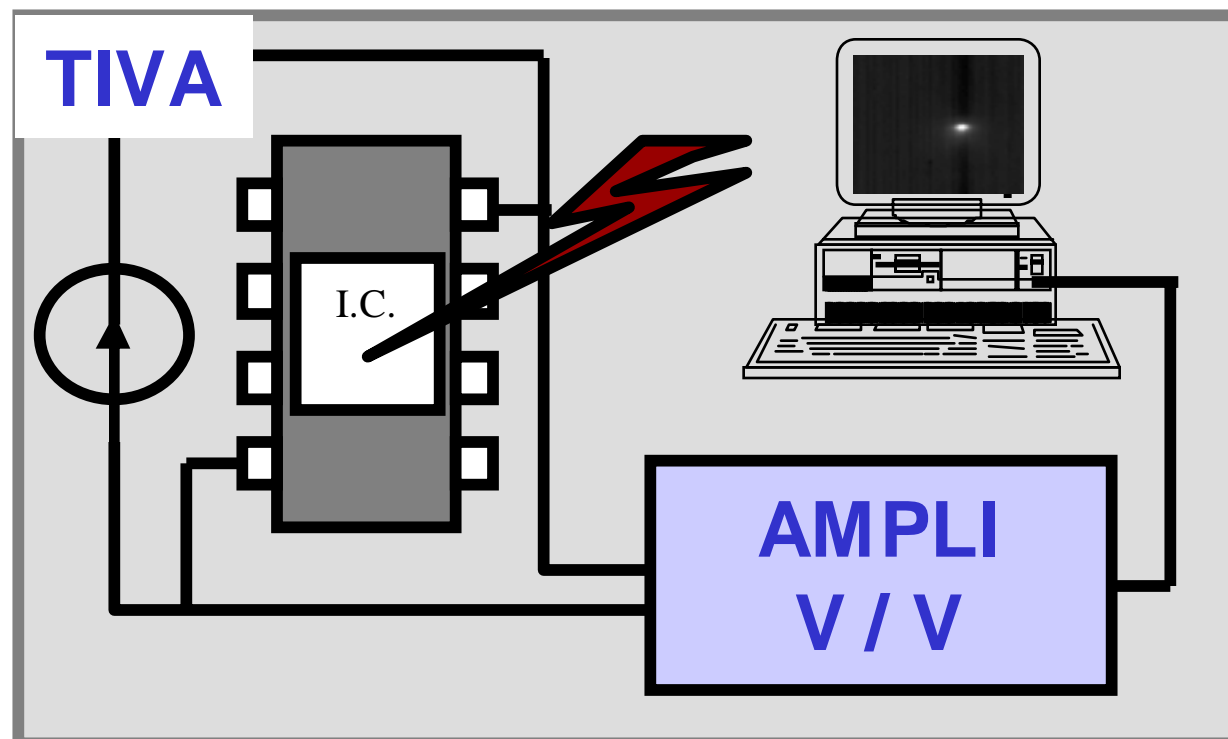
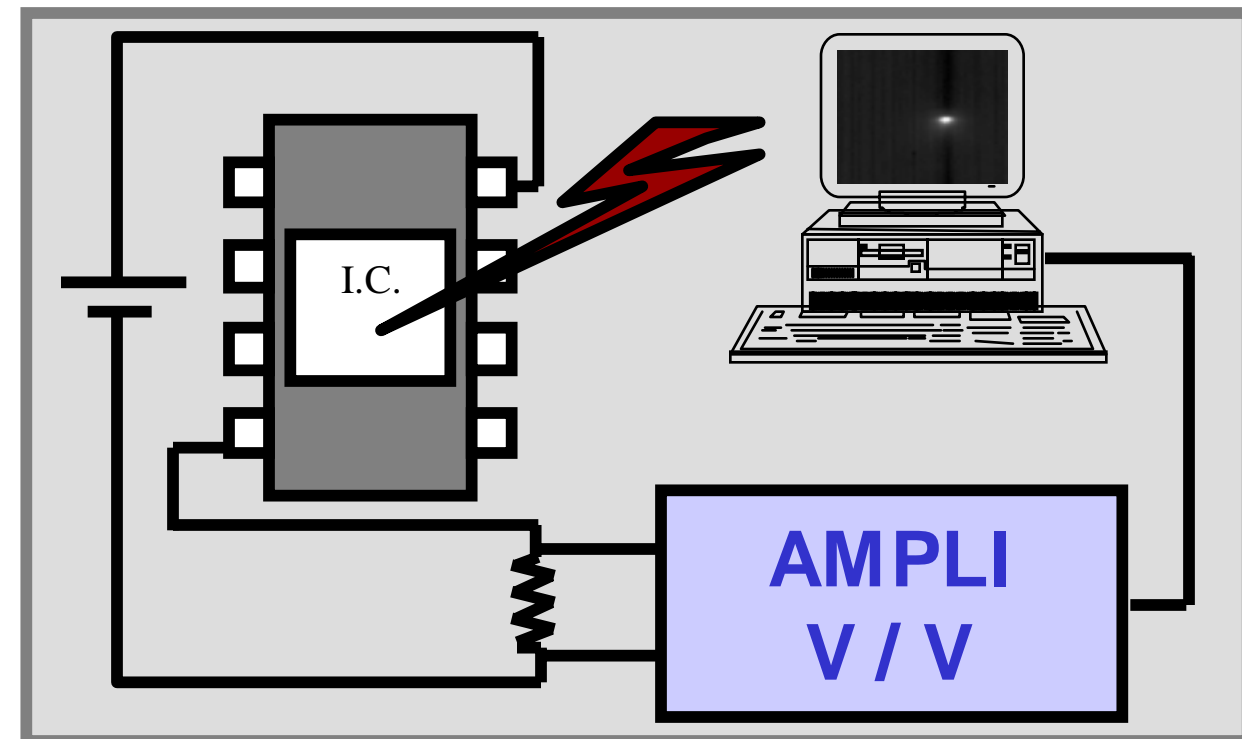
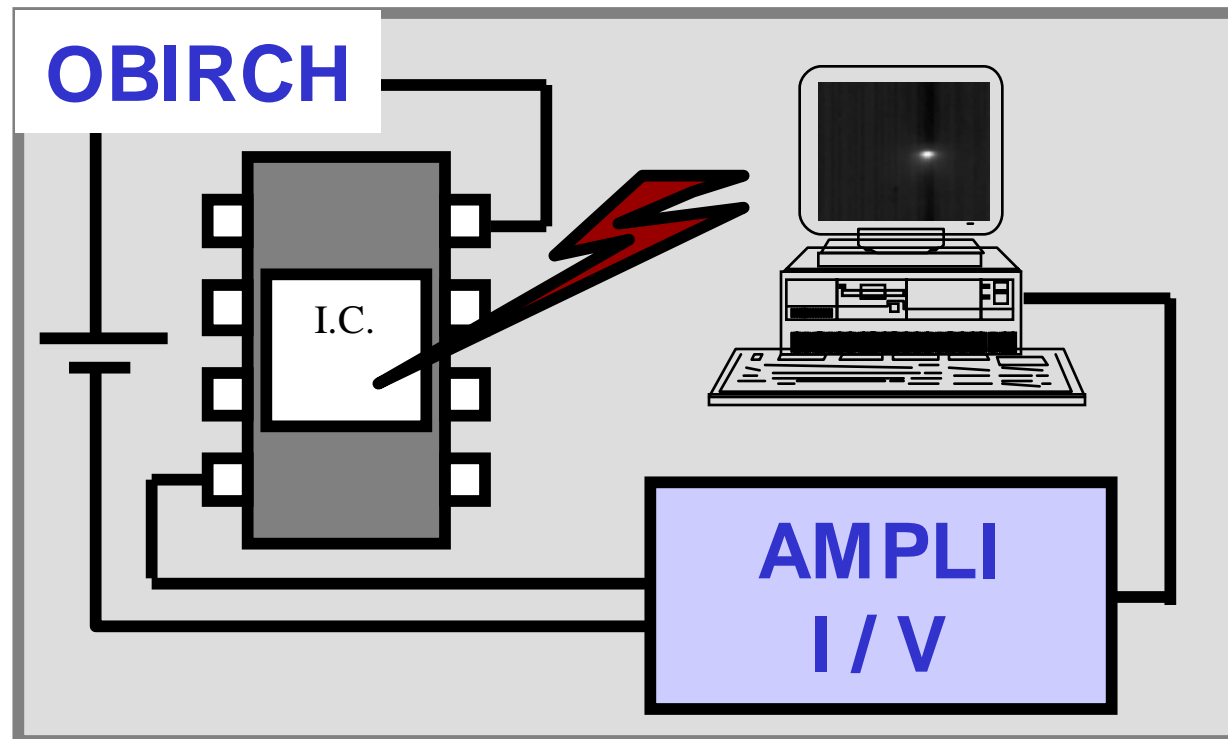
- **Laser scanning microscope (LSM)**
  - **Gaussian laser of  $\lambda > 1,1\mu\text{m}$**
- **Acquisition and imaging system**
- **Biasing and amplification scheme :**



Techniques	Inventor	Bias	Amplifier
OBIRCH	Nikawa	V	I
CC-OBIRCH TIVA	Nikawa Cole	I	V
TBIP XIVA	Palaniappan Falk	V	V
SEI	Cole	I / None	V

} TLS

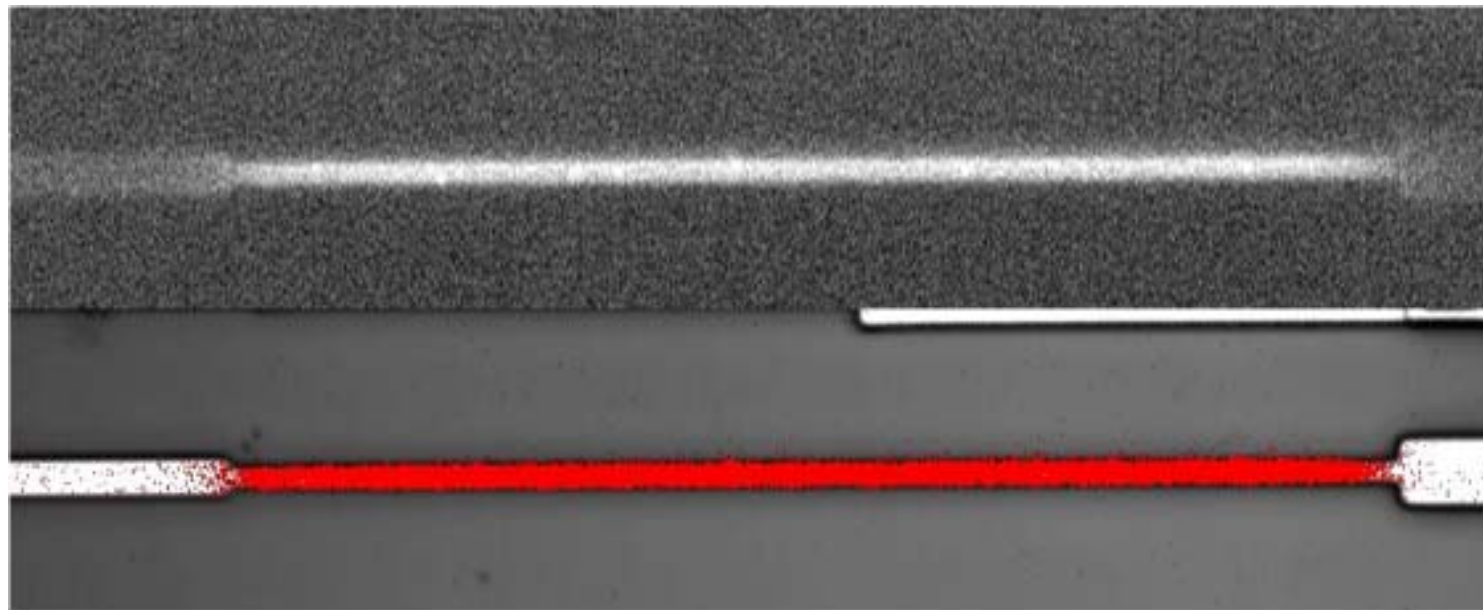
# Configurations



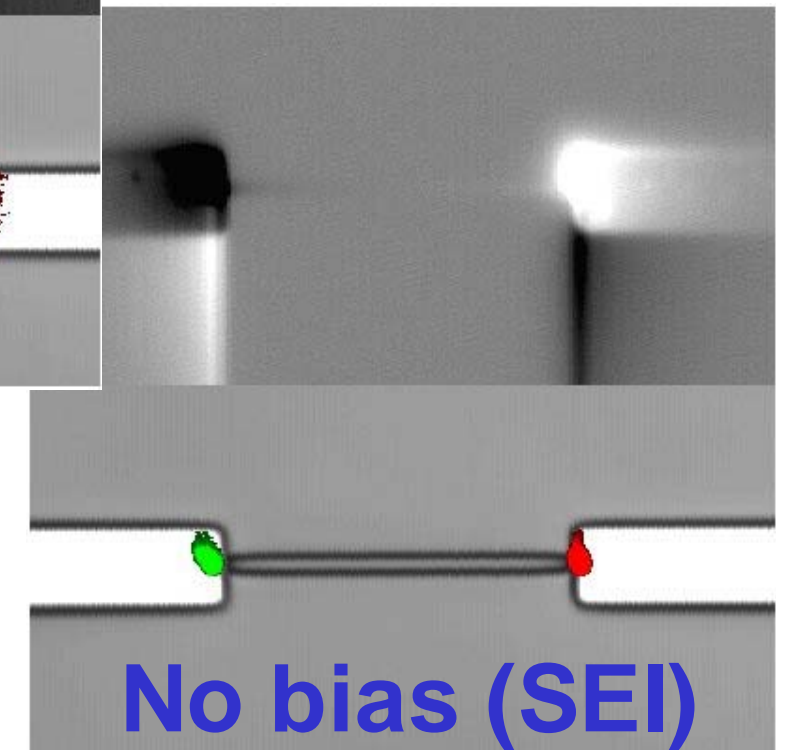
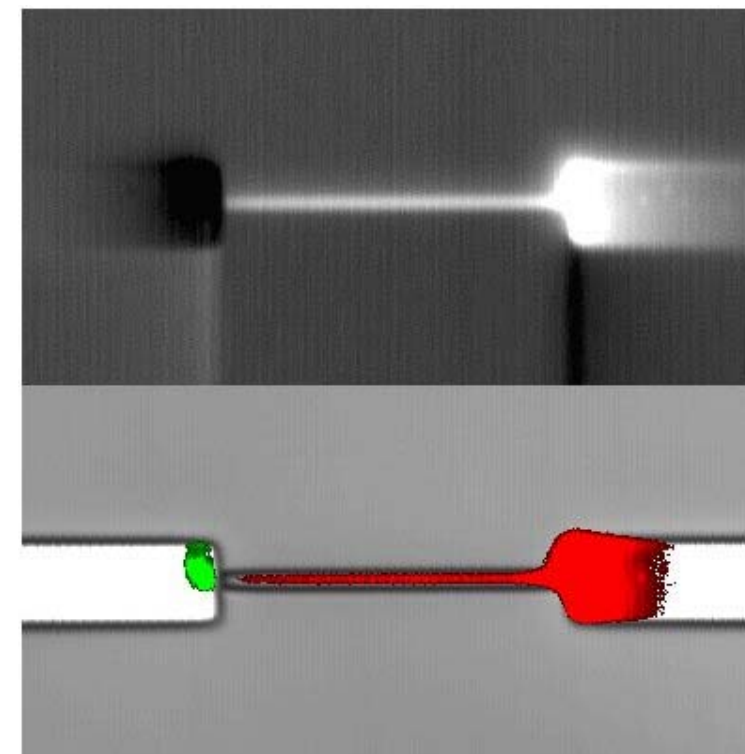
- **Other configurations:**
  - Inductance (TBIP / XIVA)
  - No bias (SEI)

# TLS on Test Structures

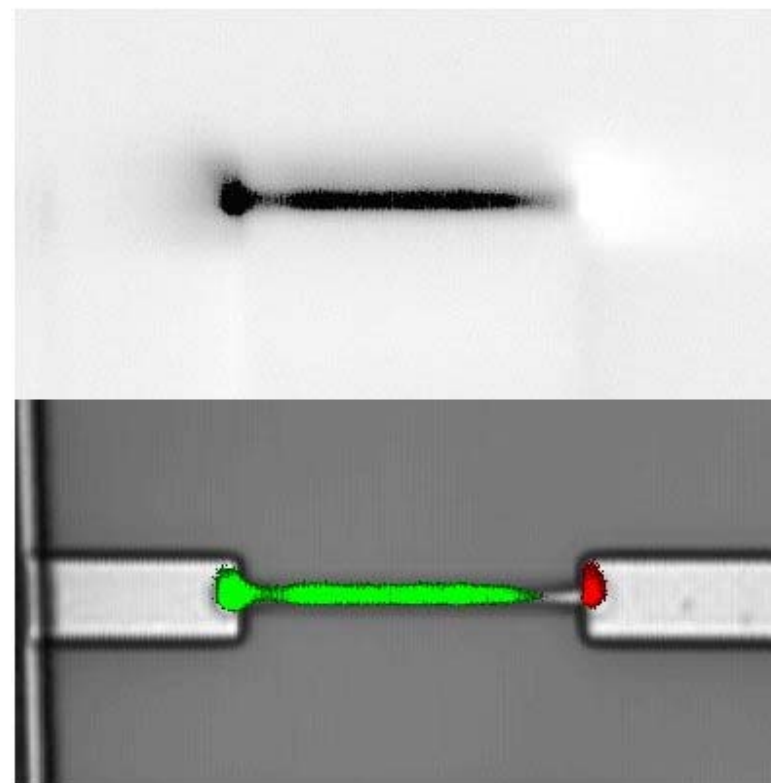
Al line



N+ resistance

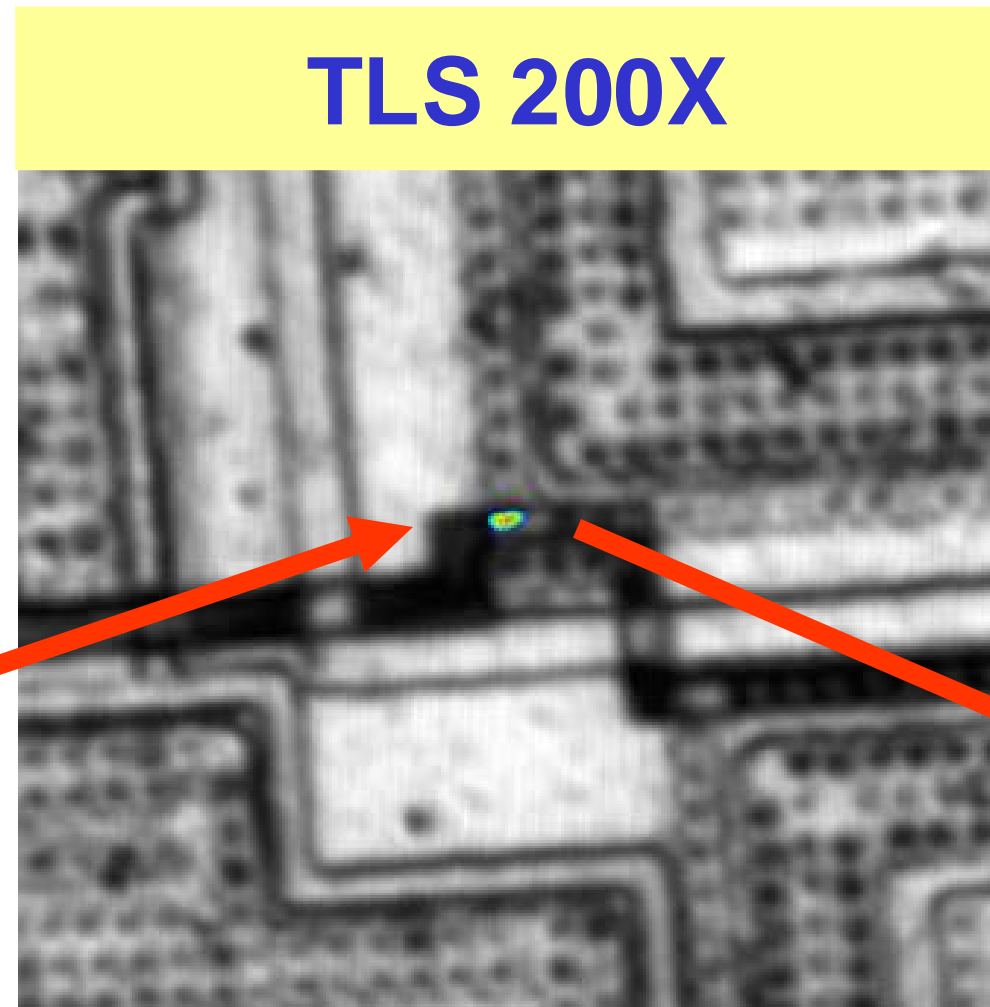
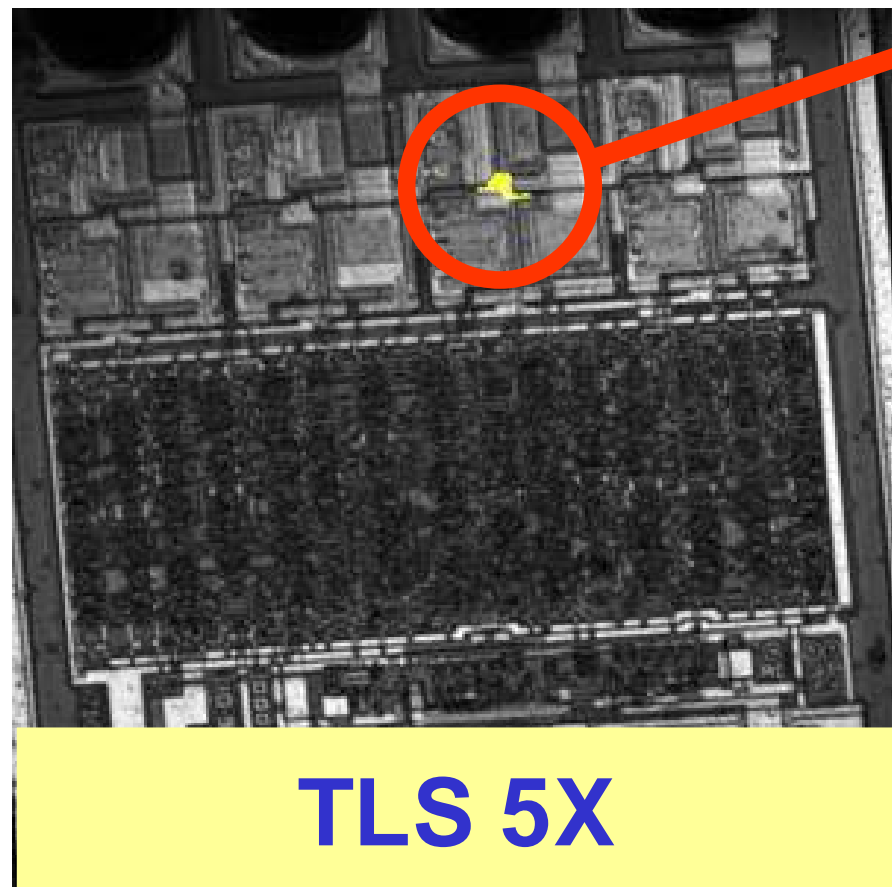


Poly line

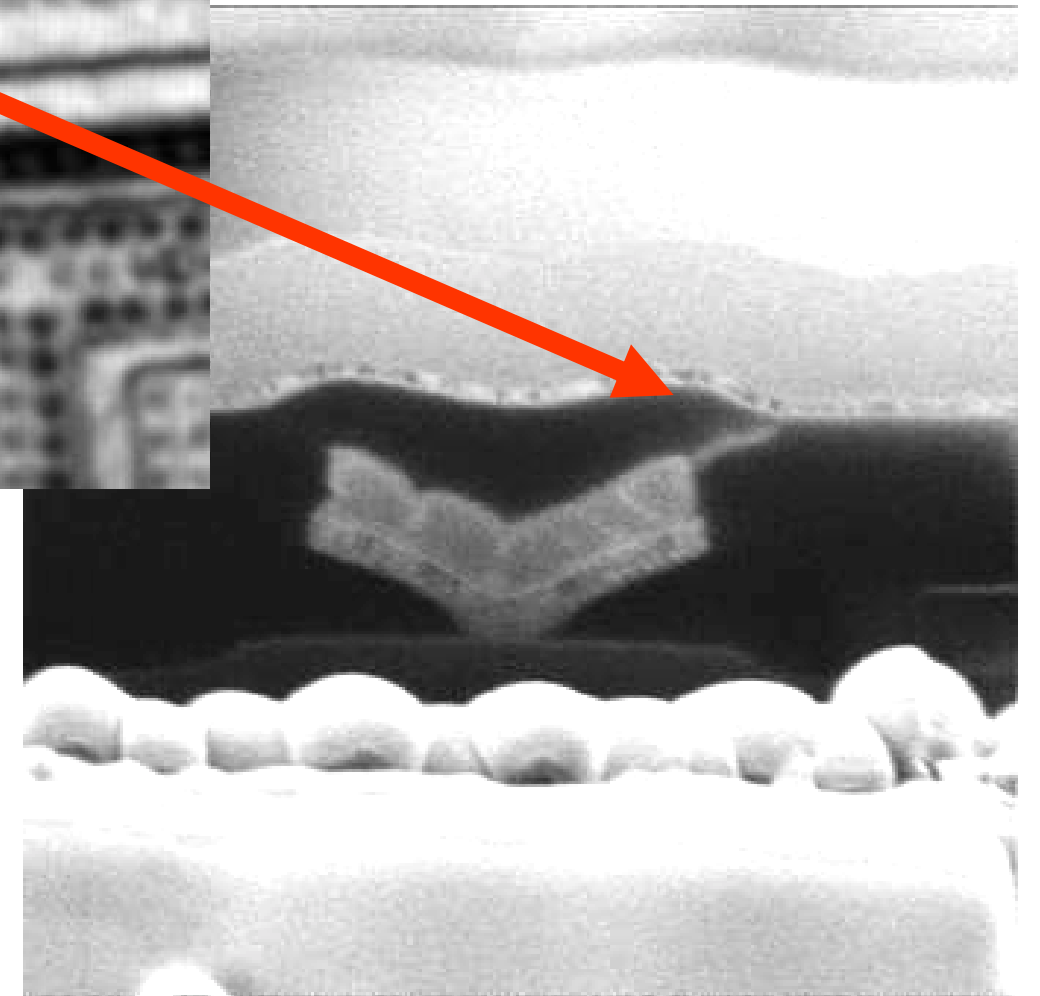


# TLS Case Study #1

- **Failed CMOS IC**
  - I ~ 2mA @ 5V
- **No emission**
- **Front-side**



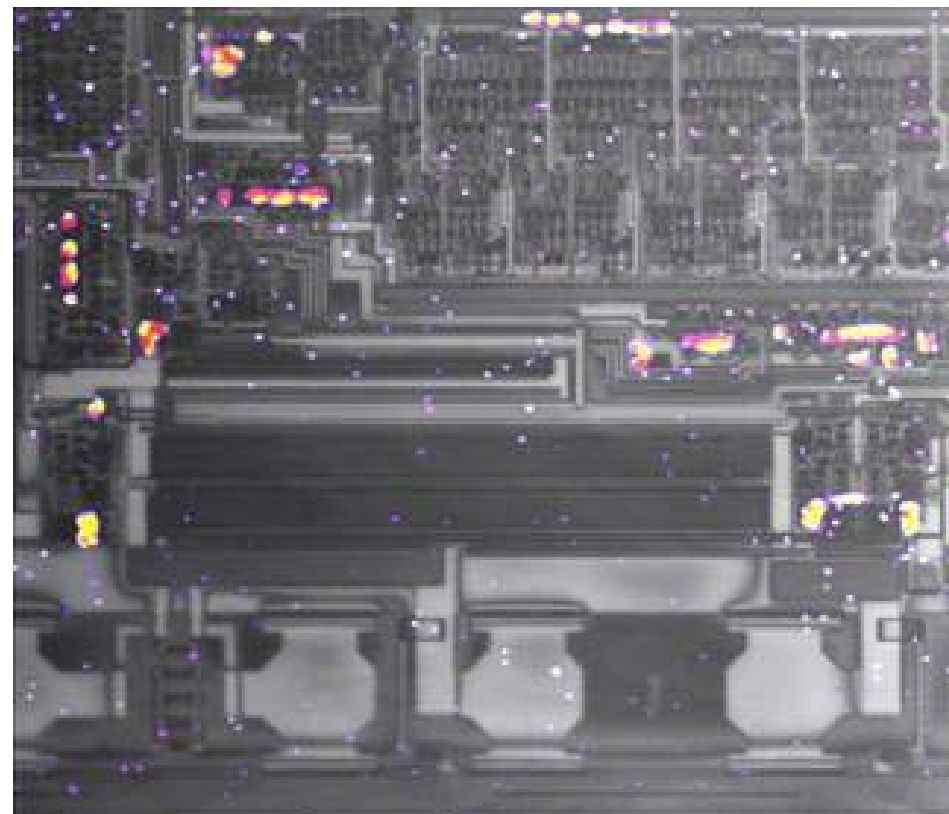
**Metal short  
(M1-M2)**



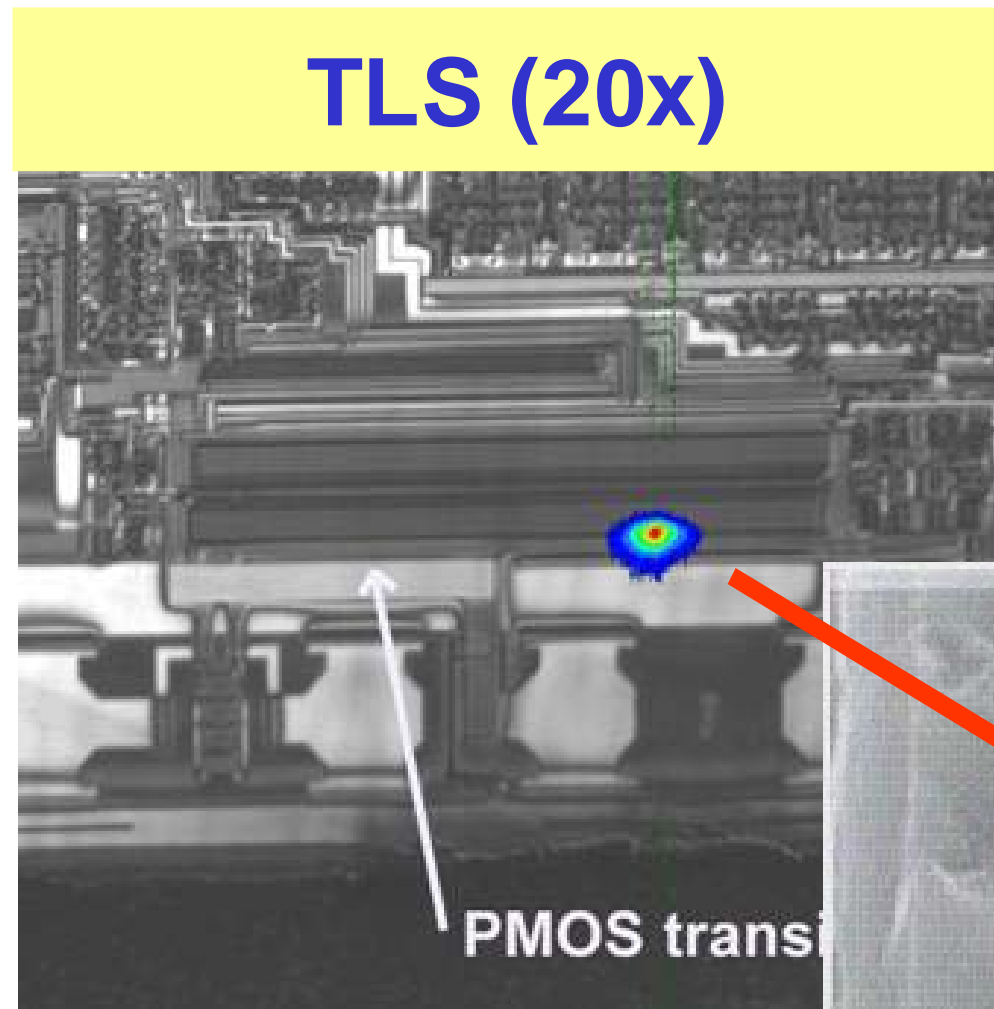


# TLS Case Study #2

- **Failed BICMOS IC**
  - $I > 100 \mu\text{A}$  (I/O)
- **Backside**
  - 4 metal levels



EMMI (20x)

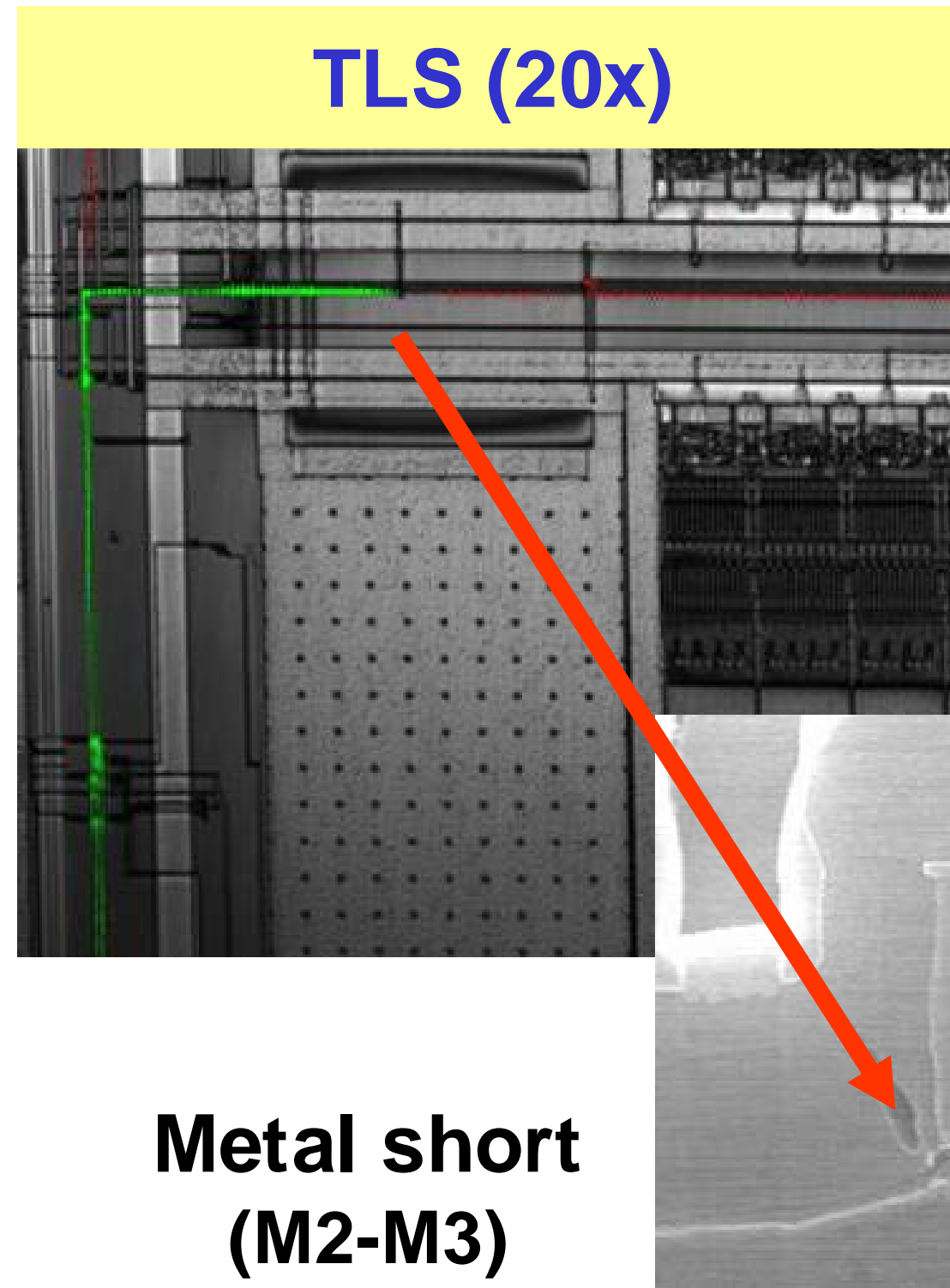
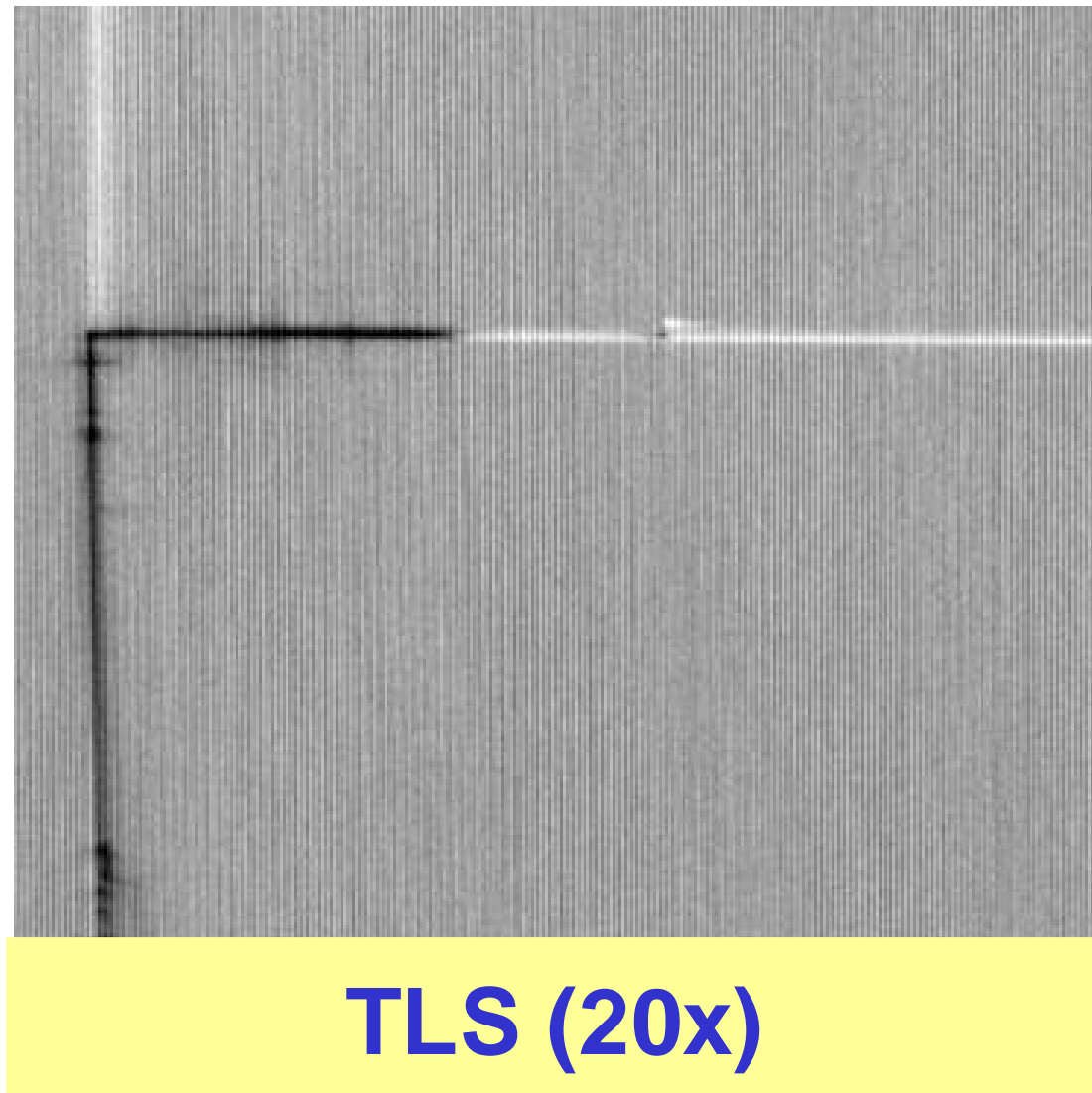


W short  
(Drain-Source)



# TLS Case Study #3

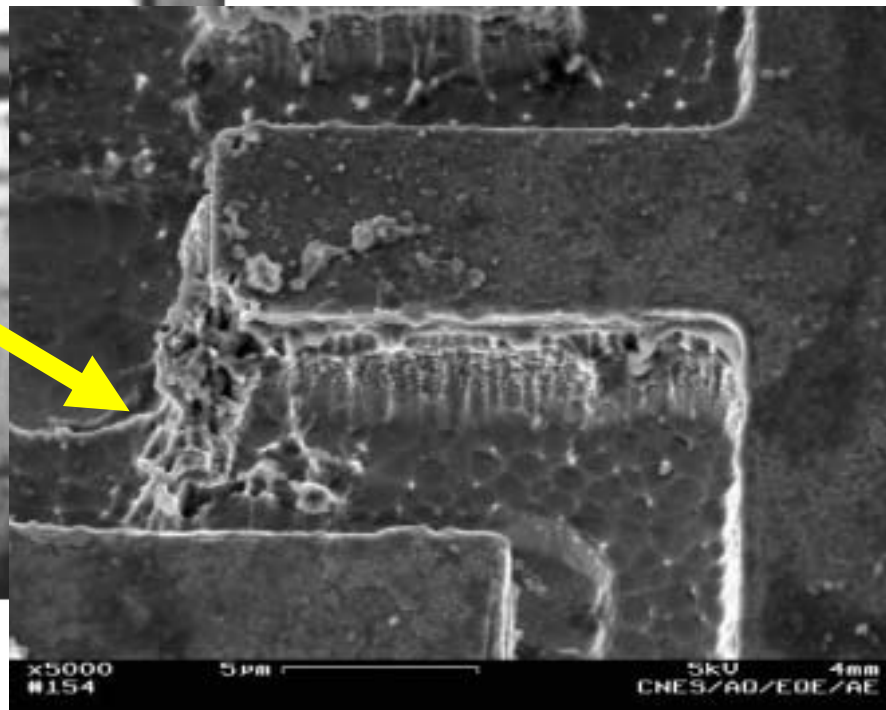
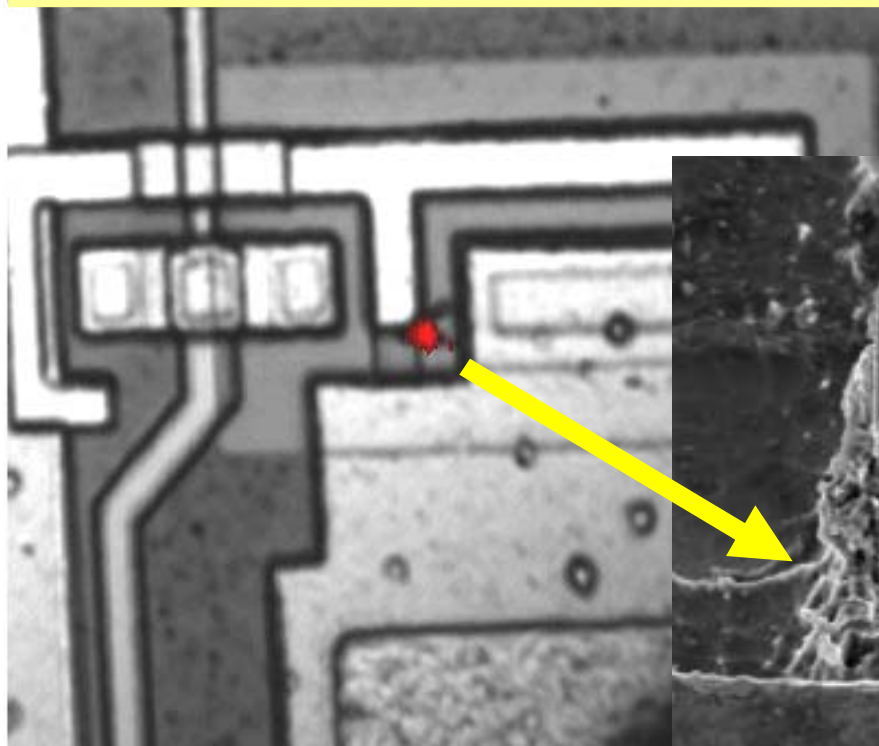
- **Failed CMOS IC**
  - I ~ 2 mA @ 3V
- **Front-side**



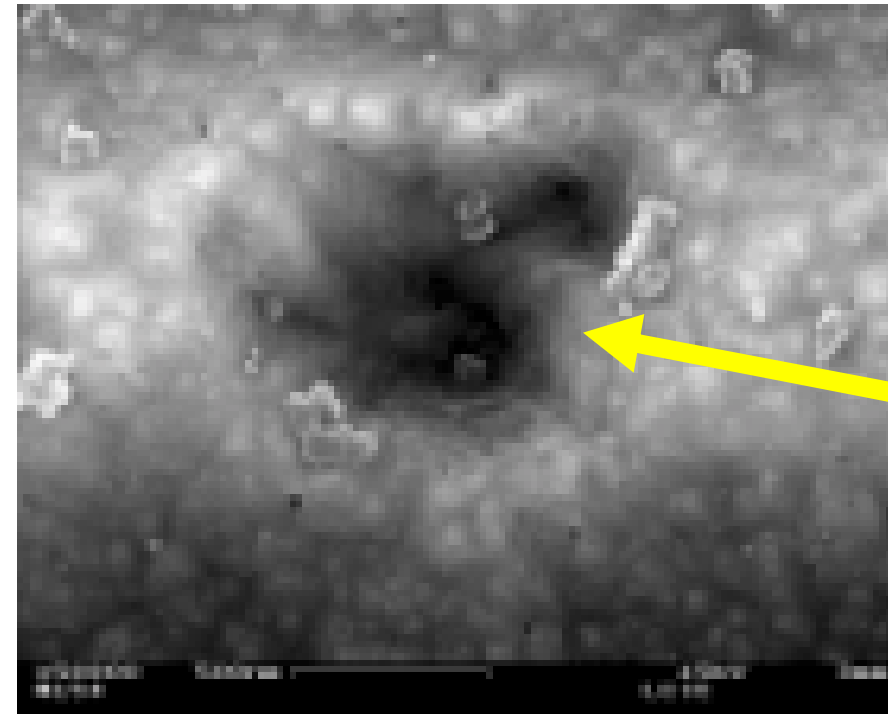
# TLS Case Study #4

- ESD failed commercial ICs
  - HBM and MM stressed
- Front-side
  - No bias applied (SEI)

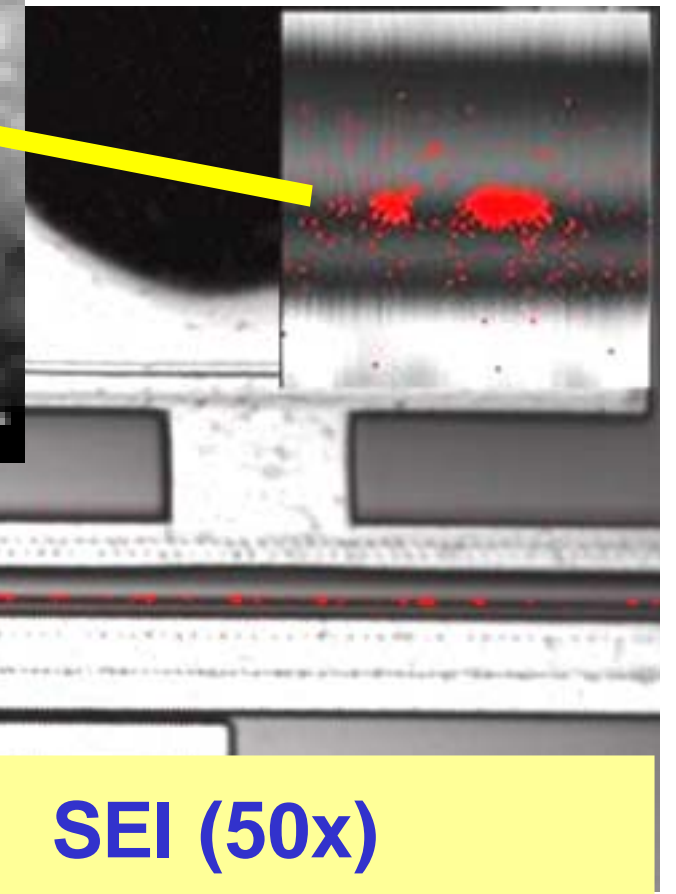
SEI (200x)



Molten Si/Al  
filament



Molten Si  
spike

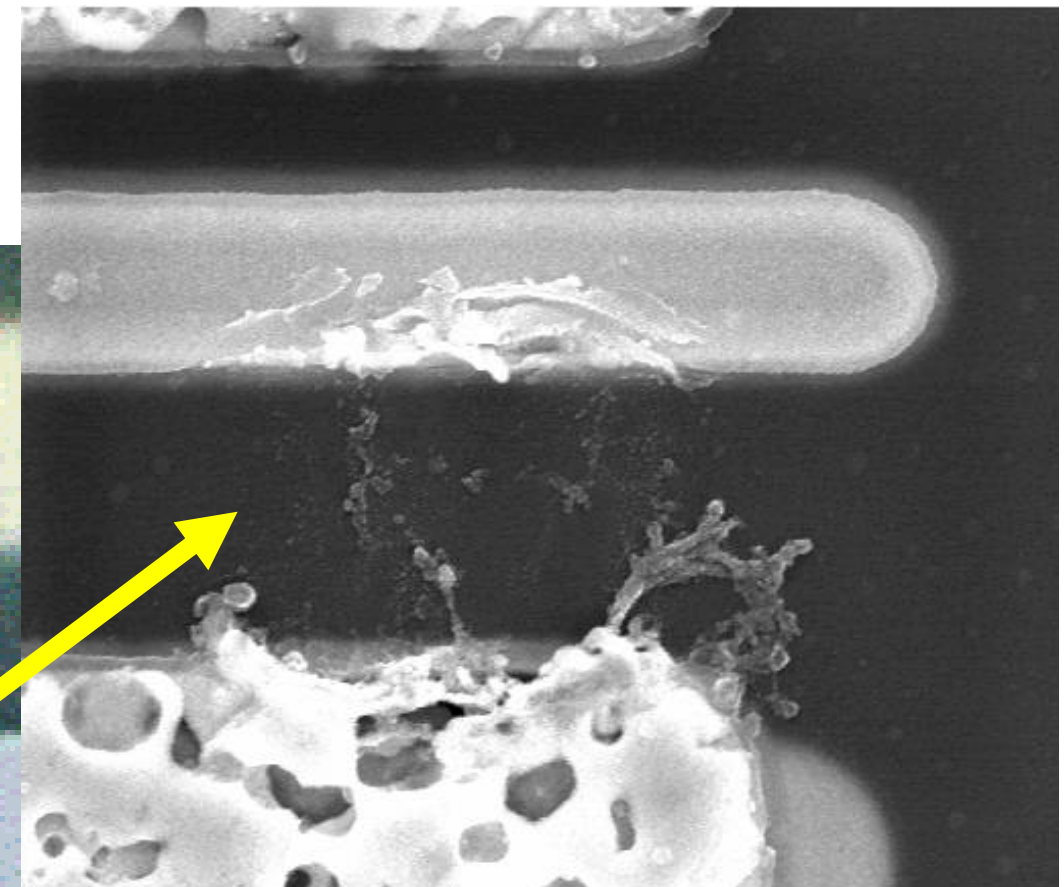
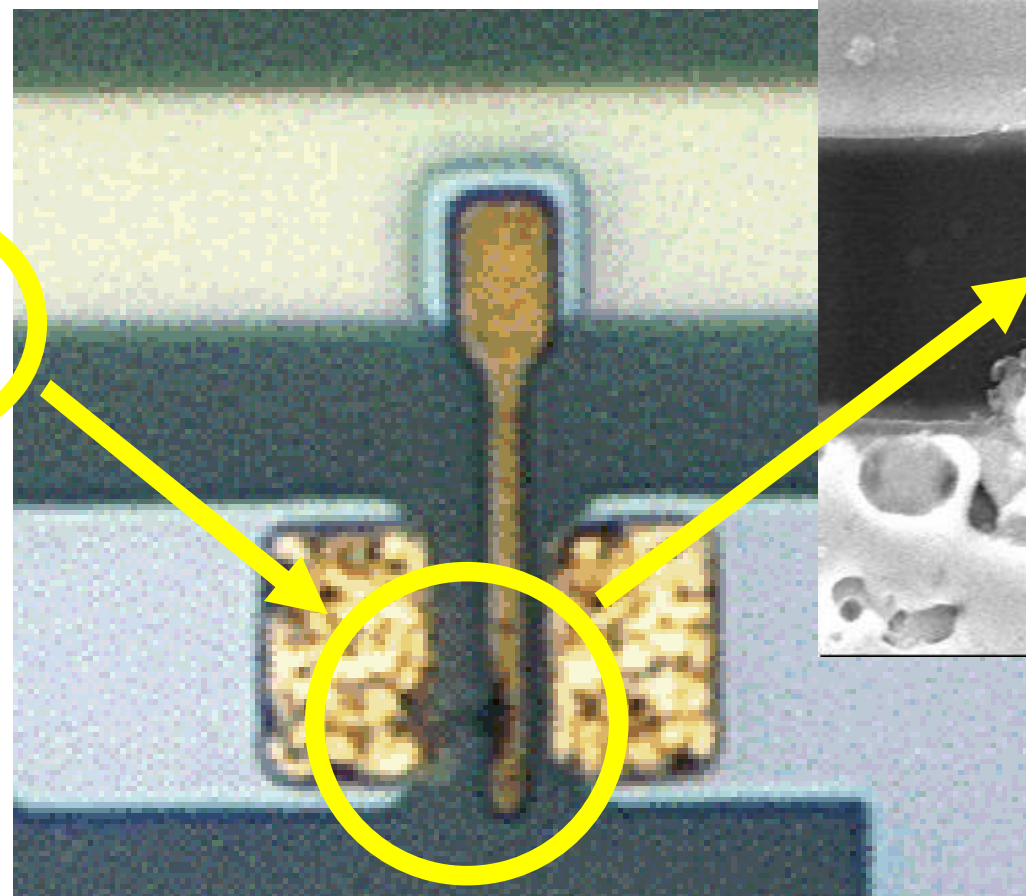
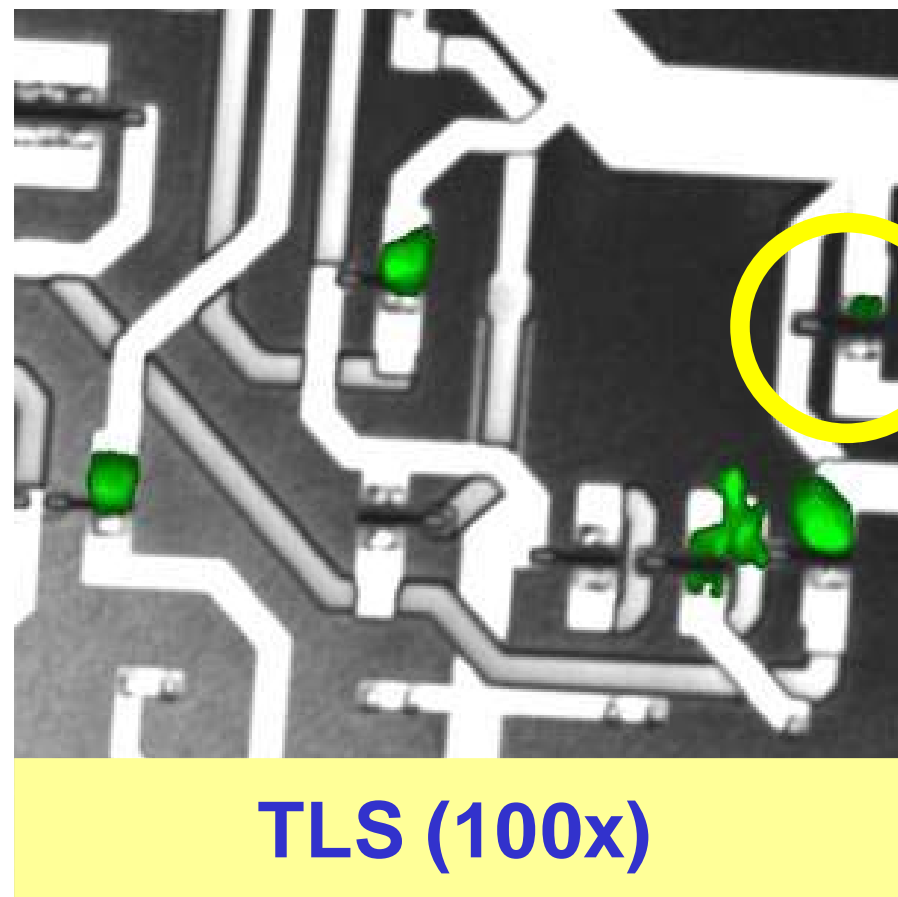


SEI (50x)

# TLS Case Study #5

- **GaAs failed ASICS**
  - I ~ 50  $\mu$ A @ 3V
- **Front-side**

Defects induced by  
CDM type ESD stress



**Gold filament**

# Conclusion : TLS Application Field

<b>Thermal Laser Stimulation</b>	<b>Signature</b>	<b>Defect type</b>	<b>Material</b>
<b>Bias</b>	<b>I<sub>leakage</sub> &gt; 1 μA</b>	<b>Current lines Shorts ESD defects Voids</b>	<b>Al, W, Au, PolySi, Doped Si, Amorph. Si</b>
<b>No Bias</b>	<b>All circuits Comparison</b>	<b>ESD defects Interface defects</b>	<b>Metal / Metal Metal / Si Metal / Poly Si Melted Si / Si</b>