Challenges and Emerging Solutions in Testing TSV-Based 3D Stacked ICs: Test Flows, Test Contents, and Test Access

Erik Jan Marinissen
IMEC – Leuven, Belgium
6. Conclusion

Summary

3D Test Flows
- A lot of potential test moments: pre-, mid-, and post-bond testing
- Test cost modeling required to determine optimal test flow

3D Test Contents
- Stay alert for new intra-die defects not covered by existing test sets
- TSV-based interconnect testing assumes controllability/observability

3D Test Access
- Wafer Probing: external test access
  - Pre-bond: fine-pitch micro-bump probing and/or extra probe pads
  - Mid-/post-bond: non-planar topologies
- DfT Architecture: internal test access
  - 3D-DfT Architecture defined
  - Part of commercial EDA tool flows, considered for standardization
6. Conclusion

References

10. Erik Jan Marinissen et al., 'Automated Design-for-Test for 2.5D and 3D SICs', Chip Scale Review, September-October 2011, pp. 18-22 (http://www.chipscalereview.com/issues/0911/)
12. Chun-Chuan Chi et al., 'Post-Bond Testing of 2.5D-SICs and 3D-SICs Containing a Passive Silicon Interposer Base', IEEE International Test Conference (ITC’11), Anaheim, California, September 2011, Paper 17.3
13. Sergej Deutsch et al., 'Automation of 3D-DfT Insertion', IEEE Asian Test Symposium (ATS’11), New Delhi, India, November 2011
6. Conclusion

Acknowledgements

- **IMEC** *(Leuven, Eindhoven)*
  3D Team + AMSIMEC + Mario Konijnenburg

- **Cadence Design Systems** *(Austin, Endicott, München, Noida)*
  Vivek Chickermane, Sergej Deutsch, Marc Greenberg, Brion Keller, Subhasish Mukherjee, Rick Schoonover

- **Cascade MicroTech** *(Beaverton, Dresden)*
  Peter Hanaway, Stojan Kanev, Jörg Kiesewetter, Axel Schmidt, Ken Smith, Eric Strid, Thomas Thärigen

- **TEL Test Systems** *(Austin, Grenoble, Kildare, Nirasaki)*
  Paul Mooney, Eric Pradel, Dan Rishavy, Don Robinson, Yoichi Shimizu

- **TUM** *(San Jose)*
  Sandeep K. Goel

- **Duke University** *(Durham)*
  Krishnendu Chakrabarty, Brandon Noia

- **National Tsing-Hua University** *(HsinChu)*
  Po-Yuan Chen, Chun-Chuan Chi, Cheng-Wen Wu

- **TU Delft** *(Delft)*
  Said Hamdioui, Mottaqiallah Taouil, Jouke Verbree
6. Conclusion

Related Events

- **3DIC**
  IEEE Intnl. 3D System Integration Conference
  [http://www.3dic-conf.jp/](http://www.3dic-conf.jp/)
  - Rotating between California, Germany, and Japan
  - Next edition: January 31-February 2, 2012 – Osaka, Japan

- **3D Integration Workshop**
  Applications, Technology, Architecture, Design, Automation, and Test
  [http://www.date-conference.com/conference/workshop-w5](http://www.date-conference.com/conference/workshop-w5)
  - Co-located with DATE’09, DATE’10, and DATE’11
  - Next edition: March 16, 2012 – Dresden, Germany (with DATE’12)

- **3D-TEST**
  IEEE Intnl. Workshop on Testing Three-Dimensional Stacked ICs
  - Co-located with ITC’10 and ITC’11
  - Next edition: November 8+9, 2012 – Anaheim CA (with ITC’12)