Addressing the Challenge of Backside Circuit Edit of Wafer Level Chip Scale Packages

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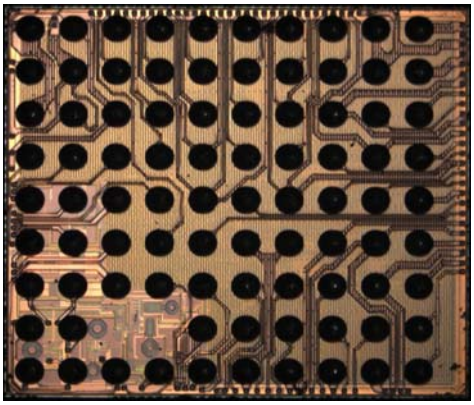
Backside edit has become commonplace at IDMs and even at some CE (circuit edit) service houses. For packaged devices only die down BGA type devices have been problematic due to access to the silicon. As can be readily understood, small die which require direct attach to a printed circuit board (PCB) may present a challenge to circuit edit. This direct use of bare die is a major trend in manufacturing electronic systems, as it decreases the number of process steps and thus reduces cost. (Die costs are generally less than a traditional package.) A package is no longer present—the die is the package (WL-CSP). Another driver to WL-CSP is the PCB real estate—smaller is better everywhere.



Example of Wafer Level-Chip Scale Package (optical image) showing <25% of the die directly accessible for editing.

The nature of wafer level chip scale packages makes them difficult to handle, not so difficult for backside circuit edit itself but for post edit functionality. In circuit edit as opposed to traditional failure analysis the goal is to make a die work again and thus the die has to be edited so that it can be tested after editing. Therefore besides the various challenges of editing, the device must be kept functional throughout the process. In our presentation we shall discuss the issues and various solutions that may address the difficulty of editing and delivering functional devices.