Localization of Electrical Shorts in Dies and Packages using Magnetic Microscopy and Lock-in-IR Thermography

M. Hechtl, G. Steckert and C. Keller
Infineon Technologies AG Munich, Germany
Phone +49-89-234-20137, Fax: +49-89-234-713752
email: martin.hechtl@infineon.com

Abstract:
Scanning SQUID Microscopy (SSM) is used to visualize current paths on package and die level.
In case studies it is shown, how the integration of SSM into the failure analysis flow and its combination with Lock-in-IR Thermography (LIT) makes it faster and allows more reliable interpretation of results.

1. Introduction

With packages getting more complex and containing more than one silicon die, the analysis flow for microelectronic devices and printed circuit boards is laying increasing stress on methods mapping hot spots and current paths on package level.

For electrical shorts, Scanning SQUID Microscopy has become the standard investigation method on package level. After first studies by Berman and Rogers in the early eighties [1] and the utilisation of high temperature superconductors for SQUID sensor fabrication [2], magnetic microscopy has gained broad access to industrial application and has been applied to semiconductor device current mapping since 1999 [e.g. 3, 4].
Moreover, high resistance defects have been investigated by SSM, e.g. damaged package vias and non-wet solder bumps [5, 6].

According to the analysis flow, a failing device is electrically tested and compared to a pass device. In case of an electrical short, SSM measurement may clarify, whether there is a short inside the package metallization, or between die pads, which should not be connected. By visualizing the shorted current path, it is possible, to compare it with the layout design and verify, whether it proceeds correctly to and from the signal and power supply die pads or bumps. The SSM result helps to locate package failures, which might otherwise have been destroyed by subsequent wet chemical decapsulation, it may support package layout descrambling and give a hint to the failure location for die level failures. For a multi-die package, by comparison of the SSM signals of pass and fail device, the failure may be attributed to a certain die.
However, in case of an SSM resolution below layout density (e.g. failure localized on die), or for rather complex current path structures, it may be difficult to localize the failure and

attribute it to a certain point of the visualized current path. This drawback may be overcome by the combination of SSM with LIT.

As an optical hot spot localization method, Lock-in-IR Thermography has shown the potential to play an important role for semiconductor failure analysis in the near future [7]. In comparison to Liquid Crystal Thermography, Emission Microscopy and TIVA, LIT is not only applicable to die level front side or backside analysis, but also for hot spots in the interposer metallization and the PCB substrate.
For an ambiguous layout situation with more than one signal path crossing the spot area (e.g. in different metallization layers) and / or current path distances closer to one another than spot resolution, it may be impossible to attribute the spot to a certain layout element, and thus identify the heat emitting structure (failure) explicitly.

Application of both SSM and Lock-in-IR Thermography combines the current path identification technique of SSM with the hot spot localization of LIT and thus makes it possible, to attribute the heat emitting structure of a failure to a certain physical feature of the failing signal path.

In this work, application results of SSM are presented for failures, which are
1) not visible in X-ray and are volatile during chemical decapsulation (lead frame short),
2) can not be attributed to a certain die by electrical testing (multi-chip module).
Moreover, example 3) demonstrates how SSM may support fault localization on die level, for defects buried under metal layers, thus invisible for optical methods like TIVA or Emission Microscopy.
Moreover, an investigation example for the combination of the two complementary methods SSM and LIT is presented, which reveals the synergetic potential achieved by the combination of the two methods.

2. Measurement techniques:

SSM is done in the failing state of a device and maps the current path, which has a short characteristic. Primarily the z (vertical) magnetic field component of a current path is measured by scanning the SSM detector along x / y direction (horizontal plane) at a certain height above the device. (For the magnetic signal, materials used in semiconductor devices

are transparent.) The resulting x / y map of the magnetic field distribution is inverted to a current distribution map by Fourier transformation. By comparison with the SSM current path image of the pass device, and comparison with package layout, the failure location may be found.

The measurement shown in this paper was carried out with a commercial Magma C20 tool from Neocera Inc. Best case values for resolution and sensitivity are about 5µm and 150nA respectively. These values, however, depend critically on the working distance between sensor and current path.

As a hot spot method, Lock-in-IR Thermography may localize a failure in a small projection area of the device. LIT is a non-steady-state technique. Thus it avoids blurring from lateral dissipation of the local hot spot thermal energy. The failing device is powered with an oscillating signal, causing time dependent behaviour of the hot spot. Only the temperature response immediately after switching on the heat source, is measured. Sensitivity to below 0.1mK and resolution up to 5µm may be achieved [8]. The actual values depend on compositional and geometric properties of the sample.

Conventional Infrared Thermography suffers from the so called emissivity problem, arising from material dependent radiation emission from the surface of heterogeneously composed samples. Due to it's Lock-in technique, LIT may display the phase image and thus overcomes the emissivity problem. A thermo camera images the surface temperature modulation dissipating from the hot spot area.

The LIT measurement in fig. 6 (as discussed later) was carried out by a TDL 384 M tool from Thermosensorik GmbH (Erlangen, Germany) [9].
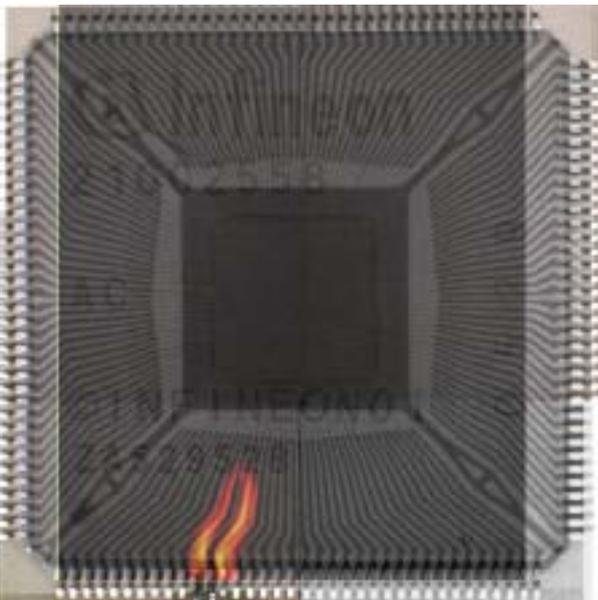

Fig.1: SSM signal, overlaid with X-ray and optical image.

3. Results and discussion

Case 1: Short in TSSOP

Most mold compounds contain hard fillers of oxide pearls. By abrasion, these filler particles may cause flaking of metallic grit from the molding compound containment during the molding process. The metallic grit may agglomerate and short-circuit package metallization. Fig.1 shows the SSM current path image (red / orange) of a fully capsulated TSSOP device, overlaid with optical and x-ray images. The current path does not reach the die, but is shorted in the lead frame area. Subsequent preparation by polishing showed, that the short was caused by iron particles (inset in fig.2) which had not been visible in previous X-ray investigation. Without SSM integrated in the analysis flow, after X-ray survey, the failing device would have been locally decapsulated, thereby removing the shorting particles with the acid. Thus the analysis would have been unsuccessful.

Fig.2: Detail of fig.1. Inset shows metallic grit, visible after mechanical polishing.

Case 2: System in Package

In a device containing seven dies, due to previous electrical characterization, malfunction was known for one of the four equivalent dies in the right half of the system (fig.3). Current mapping performed by SSM reveals, that the leakage current path is connected only with the die in the upper right corner. Local decapsulation of all four dies under suspect simultaneously would have meant a considerable risk for the package wiring in this case. Therefore, without SSM, total decapsulation, repackaging and electrical testing of all four dies under suspect would probably have been required, thus prolonging the analysis working time.
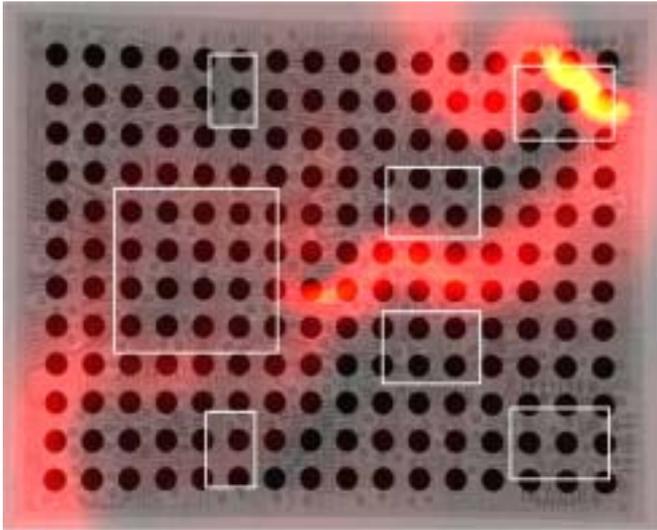
Fig.3: SSM signal, overlaid with X-ray image. Dies are outlined in white.

Case 3: ESD failure in die

SSM was carried out at a locally decapsulated device (fig.4), which had electrically failed after ESD testing. The short failure is obviously correlated with a current path reaching the die and spanning neighbouring pads. As the failure was buried under the pad metal, a previous TIVA investigation had not been successful. The small inset in fig.5 shows the ESD damage responsible for the failure, which became visible after removal of all metal layers and checking optically the ESD structures of the pads spanned by the SSM signal.
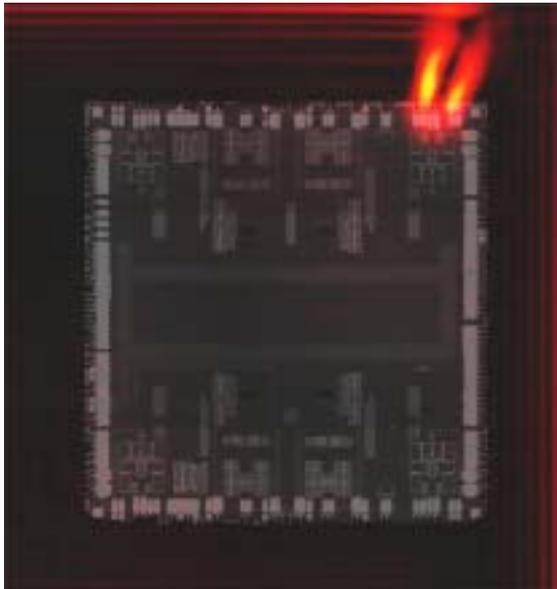

Fig.4: SSM signal, overlaid with the optical image.

Without SSM, a backside TIVA investigation would have been necessary. As in this case the package was of BGA-type, total decapsulation and repackaging would have been required. Thus, the application of SSM was much more straight forward and simplified the flow of the analysis dramatically.
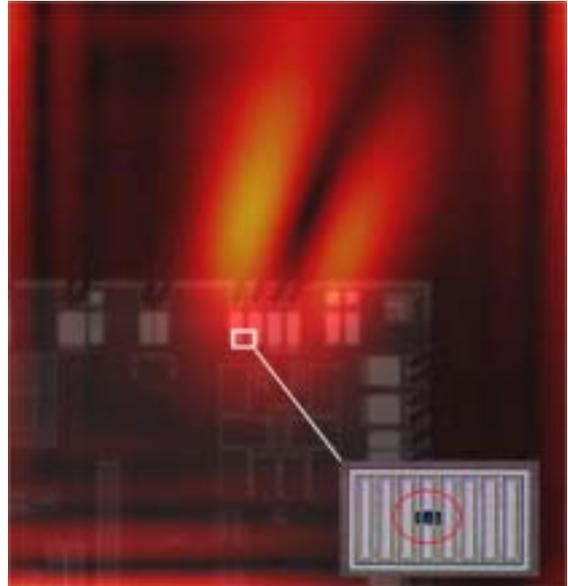

Fig.5: Detail of fig.4. Inset shows the ESD damage after lift off.

Case 4: DRAM Module

Example 4 shows a multi-chip module (fig.6) with four chips on the front side of a PCB, and four more chips on the PCB backside (the latter four chips are not visible in fig.6). After local decapsulation, electrical shorts had been built in into one of the eight chips of the module by FIB modification. Subsequently, the device was closed with a transparent pottant. In the short state the current distribution was detected by SSM. Three different current paths became visible: The upper path in fig.6 is running from one pin of the chip along the lead frame to the die leaves the chip through another pin. The second current path crosses the chip through the centre, with an additional bifurcation in the centre area. The third path appears less intensive than the previous two; it enters the chip from the lower right side, advances to the centre and becomes invisible. Using Lock-in IR Thermography, which makes very small temperature variations visible, two hot spots could be detected (right im. of fig.6). A subsequent overlay revealed, that the two LIT spots were laying on the current path and were marking the short locations.
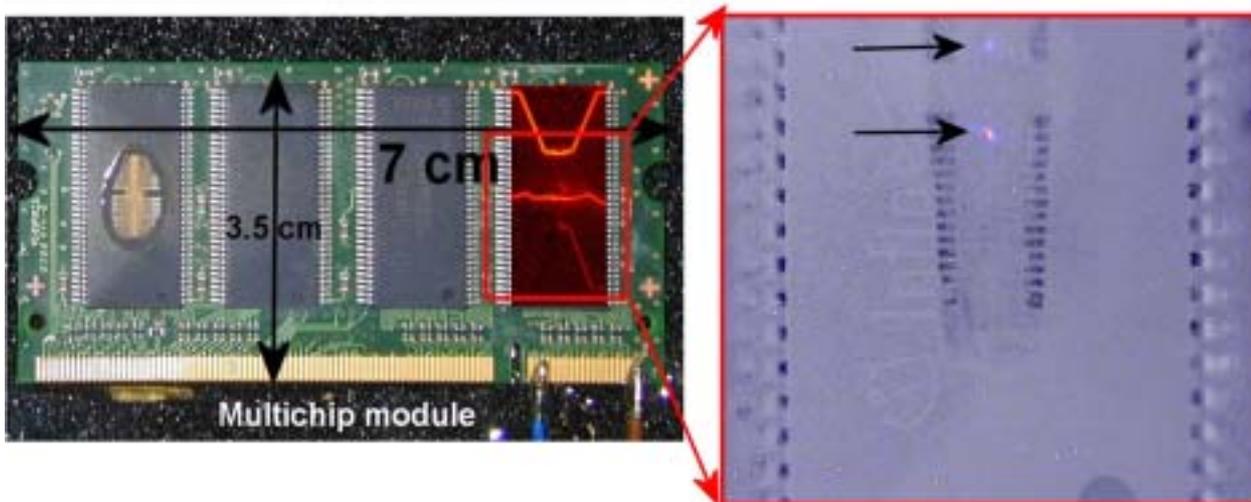
Fig.6: SSM image overlaid upon optical image (left fig.) and overlay of infrared image with optical image (right fig.).

4. Conclusion
In the near future, with increasing number of dies in one package and with higher complexity of package layout, there will be an enhanced need for qualified package level analysis tools.

In this work, scanning SQUID Microscopy was successfully employed, to clarify, whether shorts in semiconductor devices were localized in package metallization, or on die level. Package failures could be detected, which had not been visible in X-ray, and which would have been destroyed during decapsulation, without the SSM result.

For a device containing many dies, and for an ESD tested device, the application of SSM made repackaging and preparation steps for backside analysis unnecessary. Thus, the analysis flow could be shortened significantly.

The SSM current path mapping tool does not localize the hottest point on the path, which is the most probable area of a physical failure. In a case study it was demonstrated, that Lock-in-IR Thermography as a local hot spot method, is able to synergistically cooperate with Magnetic Microscopy. The measured current path defines a three-dimensional layout structure, which is connected to the failure. The hot spot emitted from a surface element of the sample, defines a one-dimensional section through the device, along which the failure will be located. The intersection of the SSM and LIT analysis results gives the unambiguous location of the physical failure.

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