SiP FA challenges

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Eufanet Workshop

SiP

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Outline

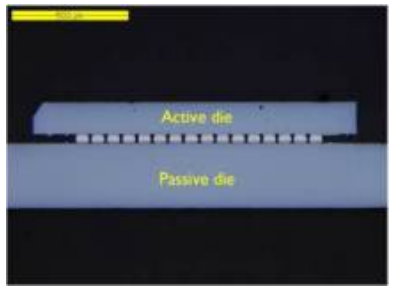
- What is System in Package?
- Benefits of a System in Package Approach
- SiP & the market
- SiP & Failure Analysis
- Failure Analysis Methodology
- Conclusion

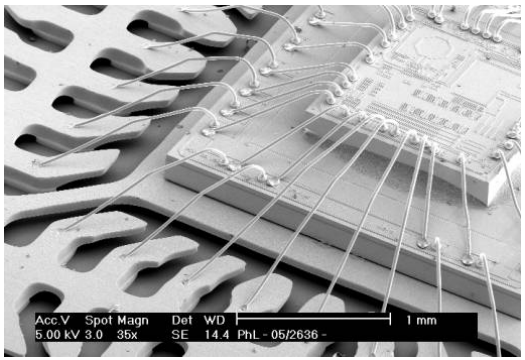
What is System in Package?

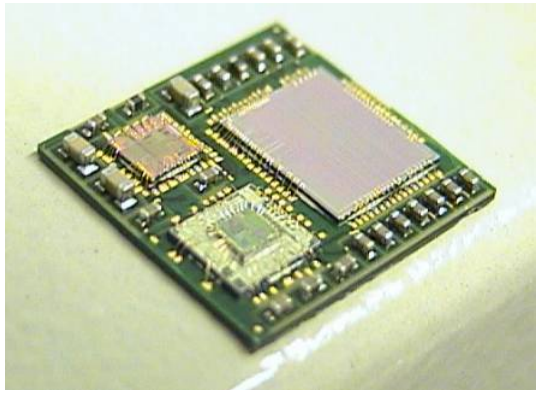
Integration of multiple dies and components, traditionally founds on the system board, in the same package to realise a fully functional system or sub-system.

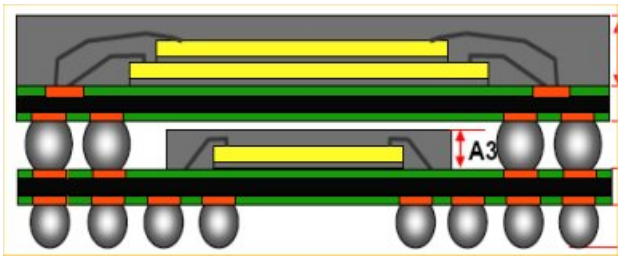
These assemblies can be made in different way:

- Dies reported on Laminate, lead-frame or silicon passive substrate
- Multi Chip Module, stack dies, single or double flip, WLP
- Package on Package
- Integration of MEMs, optical components
- Combination of all these techniques



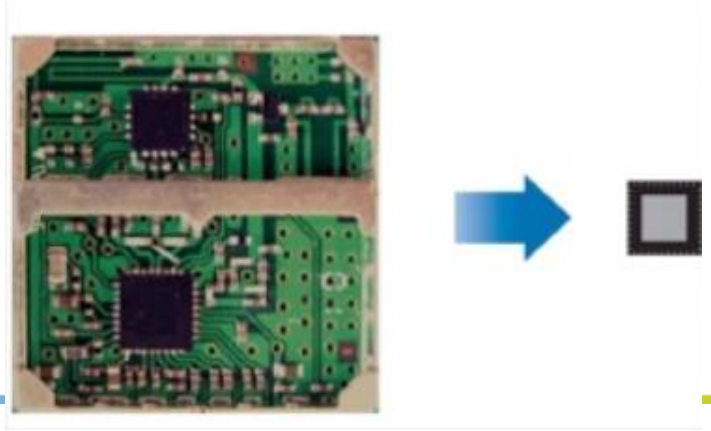






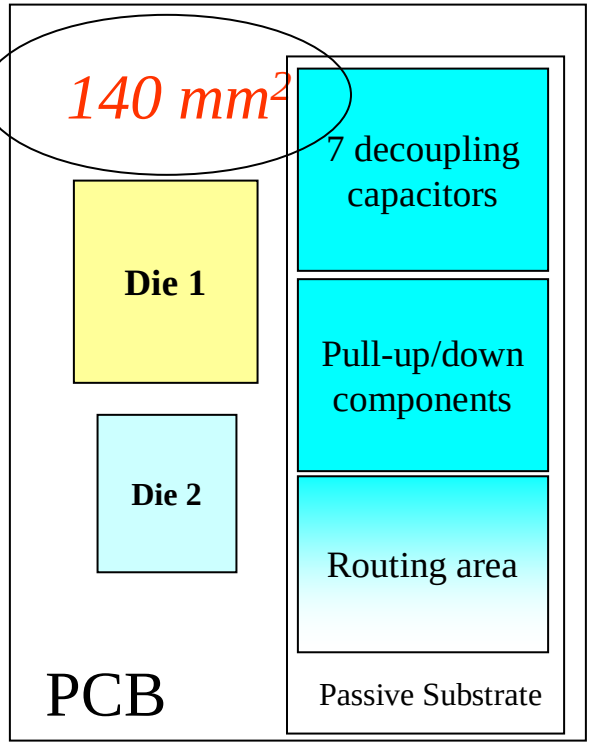
Benefits of a System in Package Approach

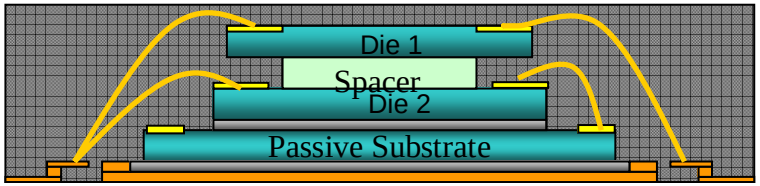
- Size reduction: SiP size is smaller than individually packaged solution
- Cost reduction : Eliminates multiple packages, simplifies board complexity, reduces size of the system board
- Performance optimisation : Shorter connexions may allow higher performance
- Complete system integration : Modular design approach, concurrrent design, more flexibility
- Fast market introduction : Reuse of existing dies, easy to mix different technologies, easy redesign vs SoC

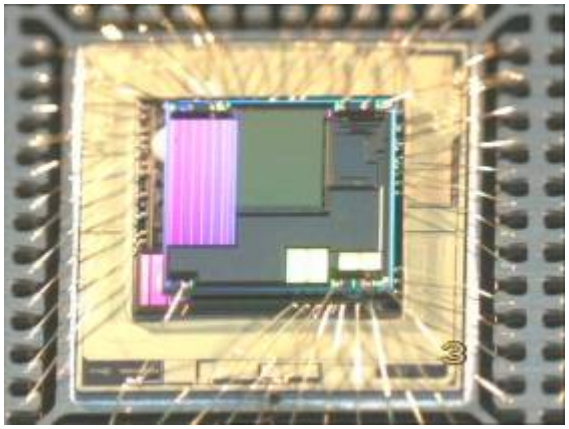


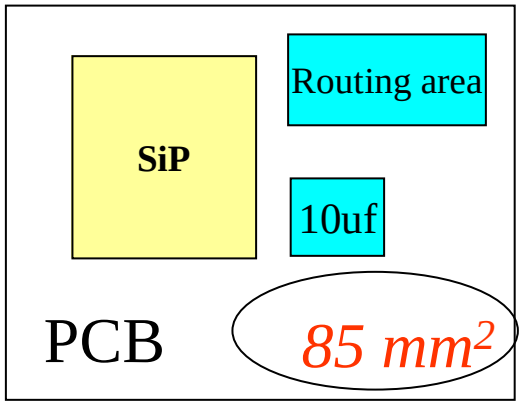
Benefits of a System in Package Approach

SiP integration Example : NFC Module





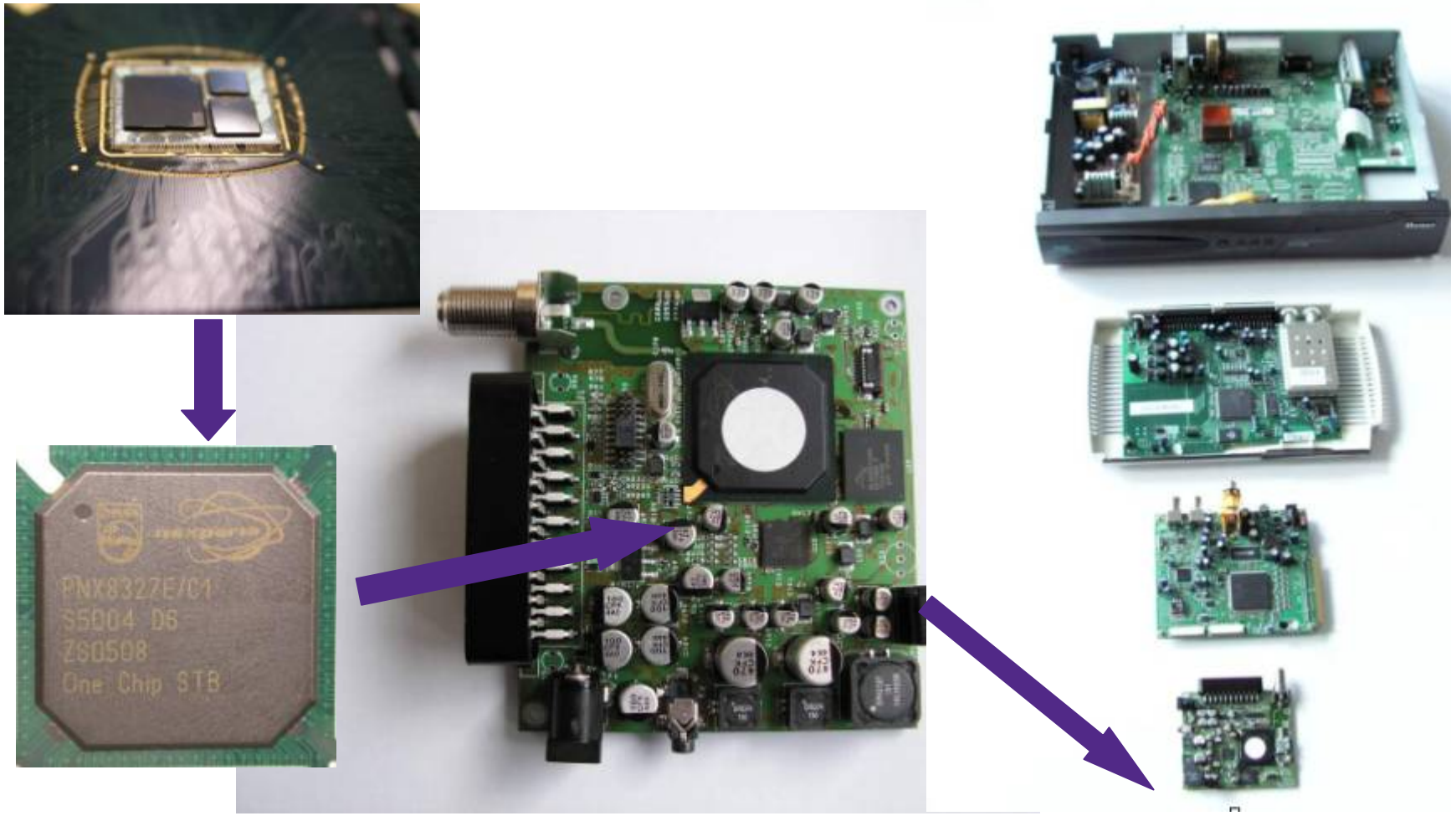




Reduction of 40% compared to a standard solution.

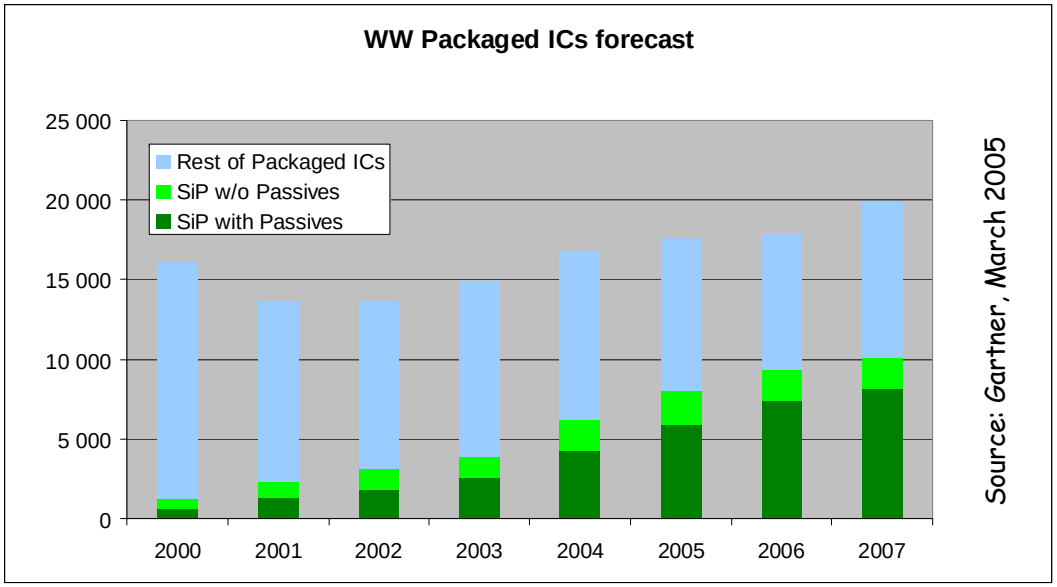
Benefits of a System in Package Approach

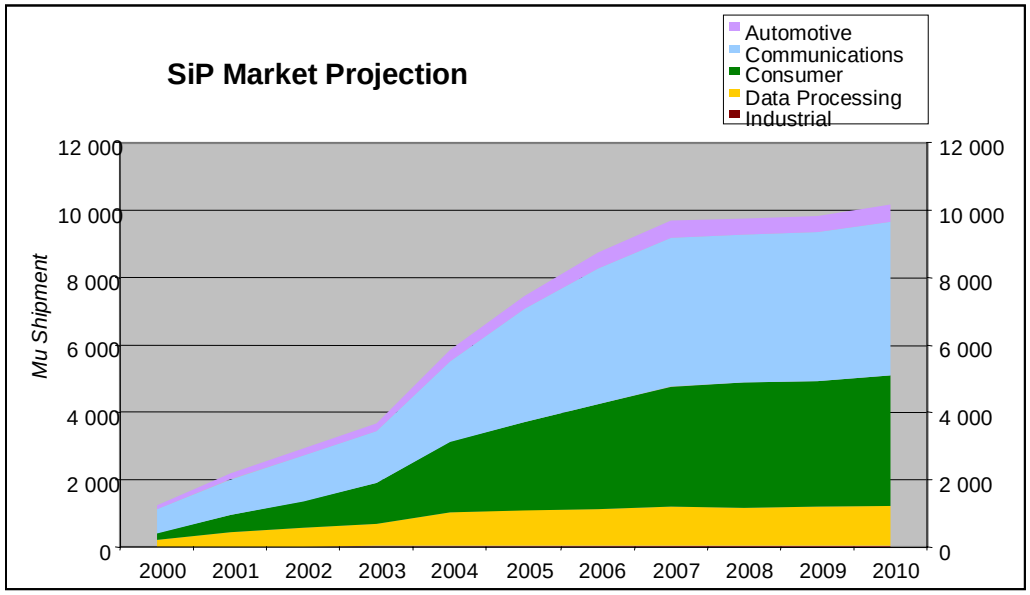
SiP integration Example : Complete Numerical TV Satellite Decoding System



SiP & the market

- **SiP market figures in 2007 from Gartner**
  - **50% ICs are SiPs** (excluding commodities and memories)
  - **80% SiPs are with passives**

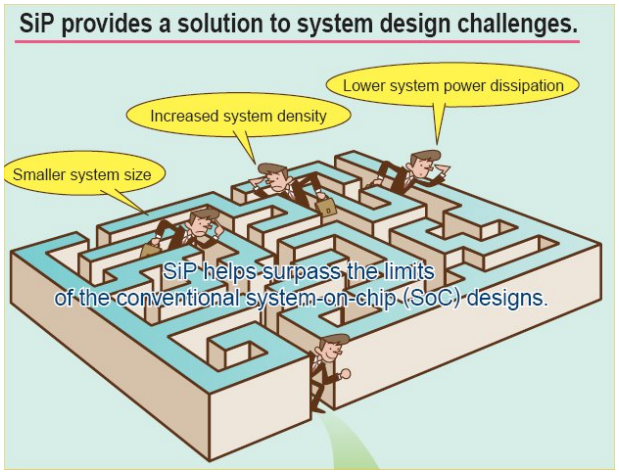


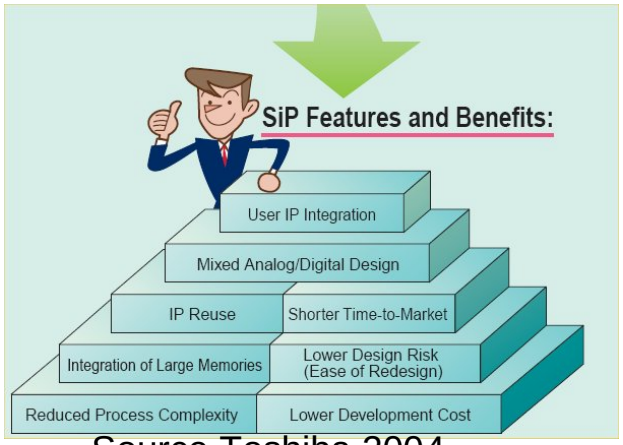


- **50% are used for Communication market**

SiP & Failure Analysis

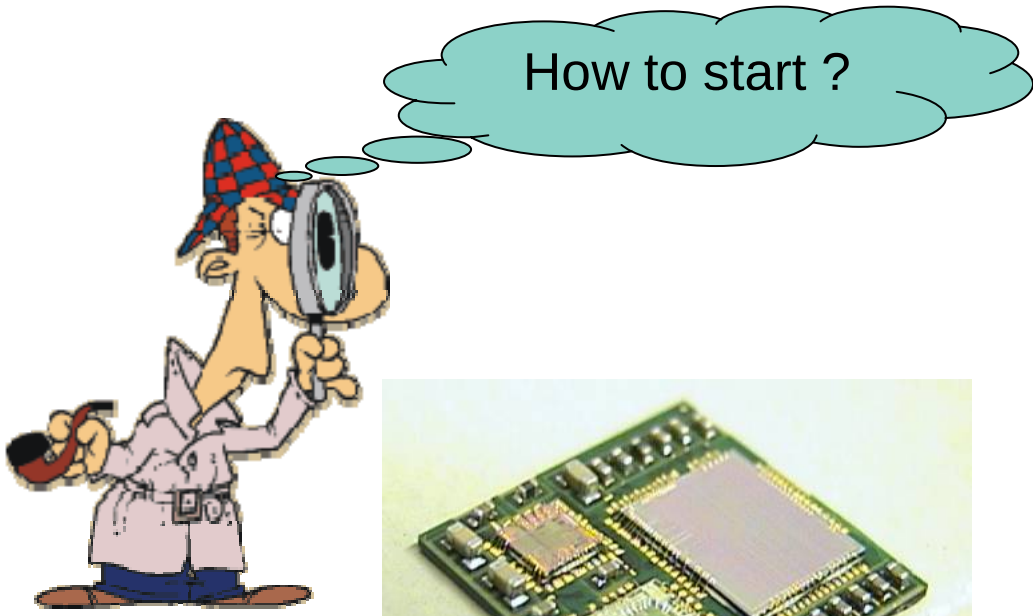
Marketing/design view





Source Toshiba 2004

Failure Analysis view



SiP & Failure Analysis

Challenges

- To identify default origin before any destructive analysis of the package : Is the defect due to the assembly or to one of the components, active or passive dies?

- To access to the failing die while keeping the whole system functional

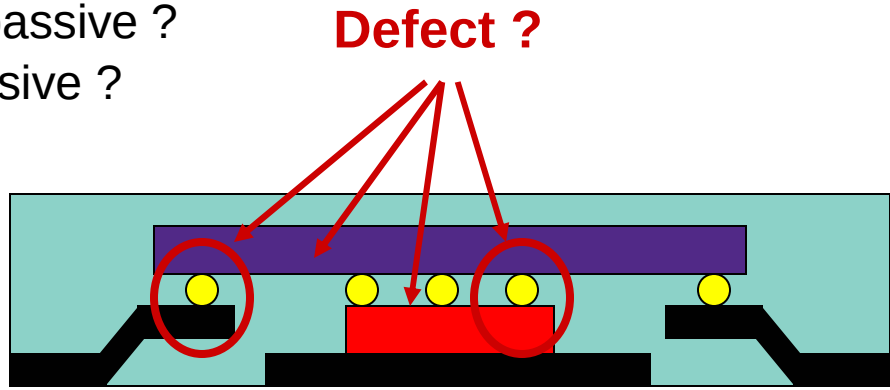
- To analyse the faulty die
  - Localise the defect within the die
  - Separate the dies
  - Re-package the die to emulate it in order to analyse it

➔ Complexity of the analysis increase with the number of components

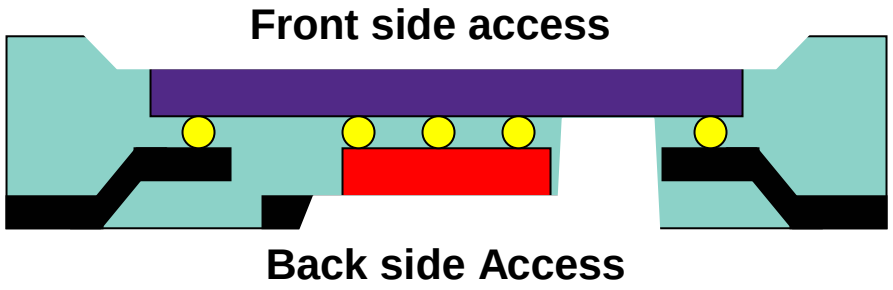
SiP & Failure Analysis

- Where does the default come from ?
  - Interconnection between package and passive ?
  - Interconnection between active and passive ?
  - Within the passive ?
  - Within the active?

➔More dies ➔ more combinations !



- Confirm and access the failing die while keeping the functionality of the complete system
  - Chemical de-capsulation
  - Mechanical de-capsulation
  - Laser ablation
  - Combination of different techniques



Failure Analysis Methodology

- Electrical Characterisation : ATE, application, I(V)
- Non destructive Analysis of assembly
  - 3D X-ray, SAM, TDR, MCI, …
- Chip access
  - Chemical, Mechanical, Laser ablation … or combination of
  - Repackaging
- Localisation Technique including stimulation of the device
  - Probing, OBIRCh, PEM, SDL, MCI, …
- Physical Analysis (often destructive): de-layering, cross sectioning, …

But the objective with SiP is ➔

Keep the system functional as long as possible and avoid altering the defect

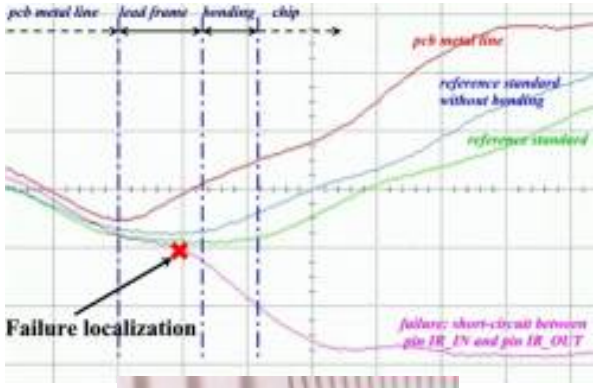
Failure Analysis Methodology

- Electrical Characterisation : ATE, application, I(V)
- **Non destructive Analysis of assembly**
  - 3D X-ray, SAM, TDR, MCI, …
- **Chip access**
  - Chemical, Mechanical, Laser ablation … or combination of
  - Repackaging
- Localisation Technique including stimulation of the device
  - Probing, OBIRCh, PEM, SDL, MCI, …
- Physical Analysis : de-layering, cross sectioning, …

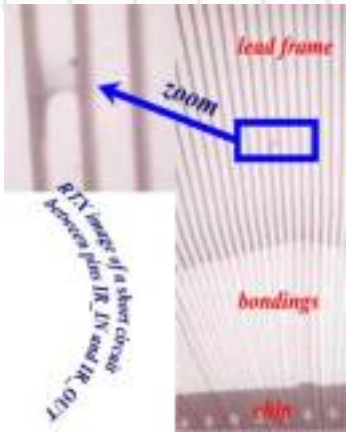
2 important points in this flow

Failure Analysis Methodology
Non Destructive Analysis

- TDR
  - Interesting technique to detect shorts or opens on LQFP and BGA.
  - Can be used to verify also line impedance.
  - Resolution is around 1mm, could reach 200um at the probe level with advanced system.



Difficulties
- Resolution becomes limited due to the need to assure a contact between the probe and the package.
- TDR for small packages is limited.



Failure Analysis Methodology
Non Destructive Analysis

- Acoustic microscopy
  - Ultrasonic examination technique can detect a lot of defects : cracks, voids, delaminations, etc.
  - It is a well known technique, lot of transducers are available with frequencies ranging from 10MHz to 200MHz and nowadays highers
  - Applicable on wafer, WLP, etc.

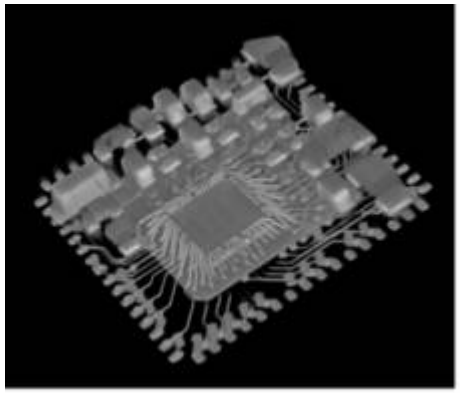
  Difficulties
  - The higher the scanning frequency, the higher the resolution but the lower the depth of analysis
  - With SiP, echo's analysis becomes more difficult due to the closely interfaces in packages with multiple stacked dies.
  - Die edge detection becomes also a difficulty.

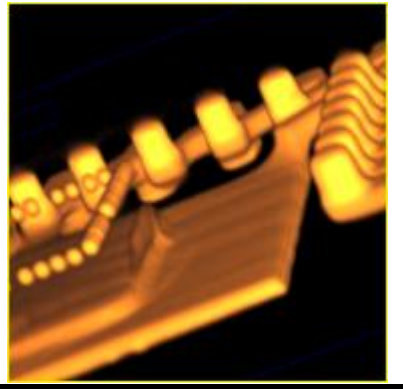
Failure Analysis Methodology
Non Destructive Analysis

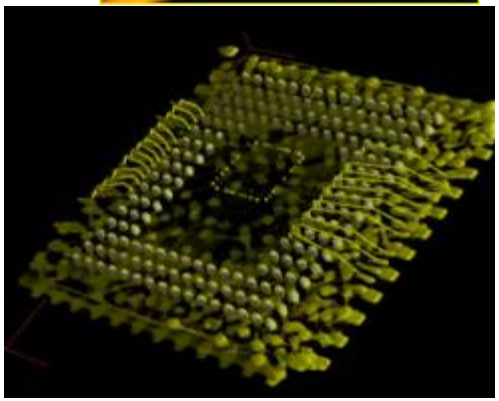
- 3D Xray Tomography
  - Very interesting technique with micronic resolution.
  - This technique allows to identify lots of assembly problems due to the ability to perform virtual cross sectioning, planar grinding and delayering.
  - Simpler analysis of complex geometries of multi layer stacks and materials resistant to X-ray penetration (thick Cu heat sinks, dense solders, …)

Difficulties

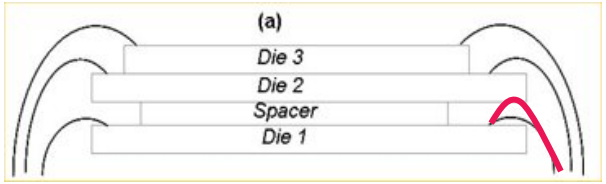
- May be a little bit time consuming.
- As the resolution depends on the distance of the sample to the X-ray source, it is less useful with packages on board.





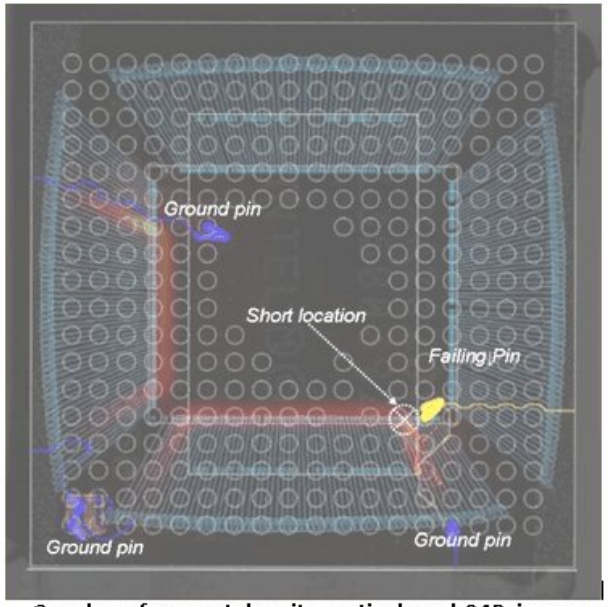


Failure Analysis Methodology
Non Destructive Analysis



- Magnetic current imaging
  - This powerful technique could be used at package level for shorts, high-resistance defects.
  - Also applicable at die level.

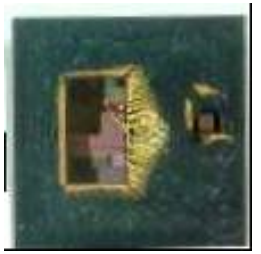
Difficulties
- Device needs to be powered up.
- Resolution depends on the distance between the sensors and the defects, more distance induce less resolution.



Overlay of current density, optical, and CAD images in triple-stacked die package with electric short failure mode

Source Intel Technology Journal, volume 9, issue4, 2005

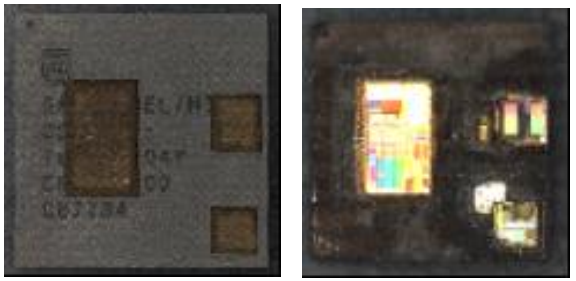
Failure Analysis Methodology
Chip access



Chemical de-capsulation

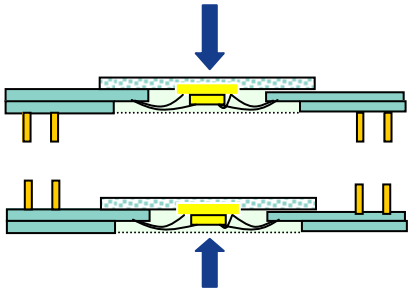
Chip access and repackaging

- Chemical, Mechanical, Laser ablation, …
  - Due to the size of the different dies and their location within the package, laser ablation combined with chemical is a good solution
  - Laser ablation, alone, is not yet possible ➔ Die destruction

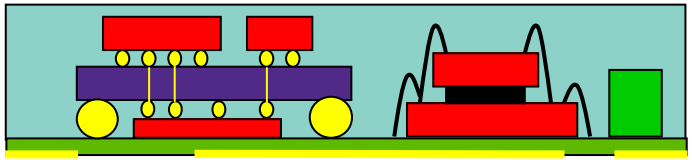


Laser + Chemical

- Repackaging
  - Many solutions exist but generally need time (day) to be prepared for analysis.



Conclusion



- Techniques
  - All these techniques describe still need improvement to fulfil SiP requirements.
  - Other techniques need to be studied: Advanced thermal Imaging, Laser spallation, …
  - Test methods like non contact tests to allow access to one specific die could be useful.

- New failure mechanisms
  - Interaction between the different dies : coupling, EMC, …
  - Reliability of new assemblies : WLP, silicon thickness, Thermo-mechanical stress, …
  - MEMs and Optical components, …

- Chip access
  - Disassembly of SiP systems without altering the defect or causing artefacts
  - Repackaging solutions to test individual die in the complete system

- Analysis complexity
  - Analysis complexity will induce an increase of the analysis time, often incompatible with customer requests.
  - Cost of new equipments.