credence

4 October 2006

Addressing the Challenge of Backside Circuit Edit of Wafer-Level Packages

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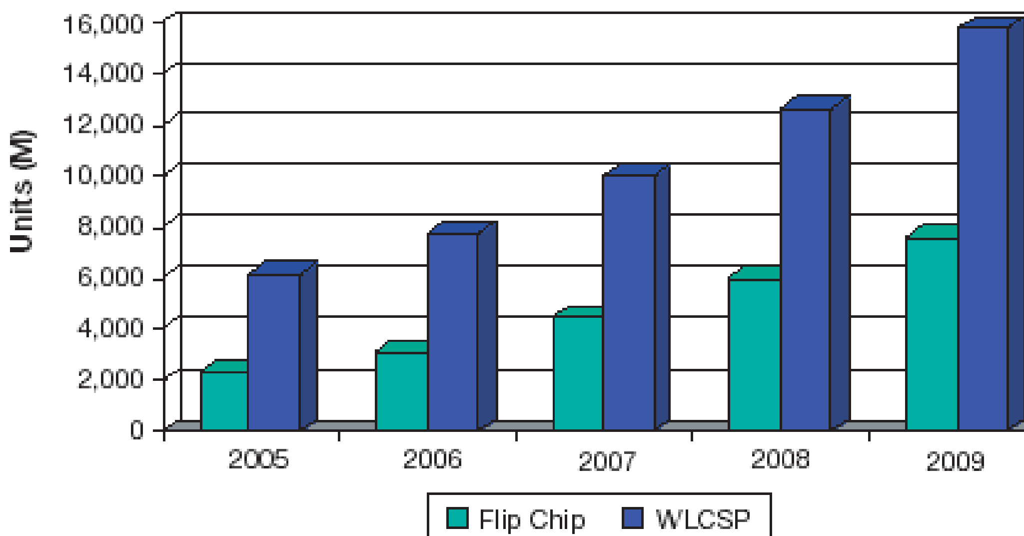
ESREF-EuFANet 2006, Wuppertal, Germany

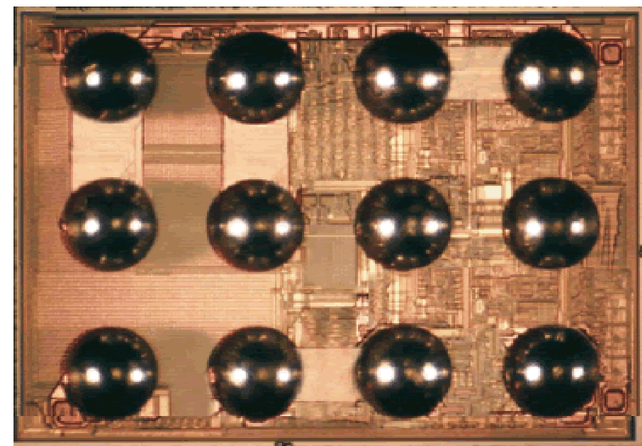
Motivation:

- Die down PCB attachment is the trend
  - Reduces cost (decreases process steps)
    - No package—die is the package → WL-CSP
  - PCB real estate valuable—smaller is better everywhere
- < 40% of WL-CSP die accessible
  - FS-CE restricted by 1) balls/pads, 2) redistribution layer (RDL), 3) protective & passivation layers
  - Backside CE

Die Size (mm)	Balls in Array
1 x 1	2 x 2
2 x 2	4 x 4
3 x 3	6 x 6



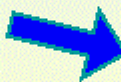
Wafer Level-Chip Scale Package

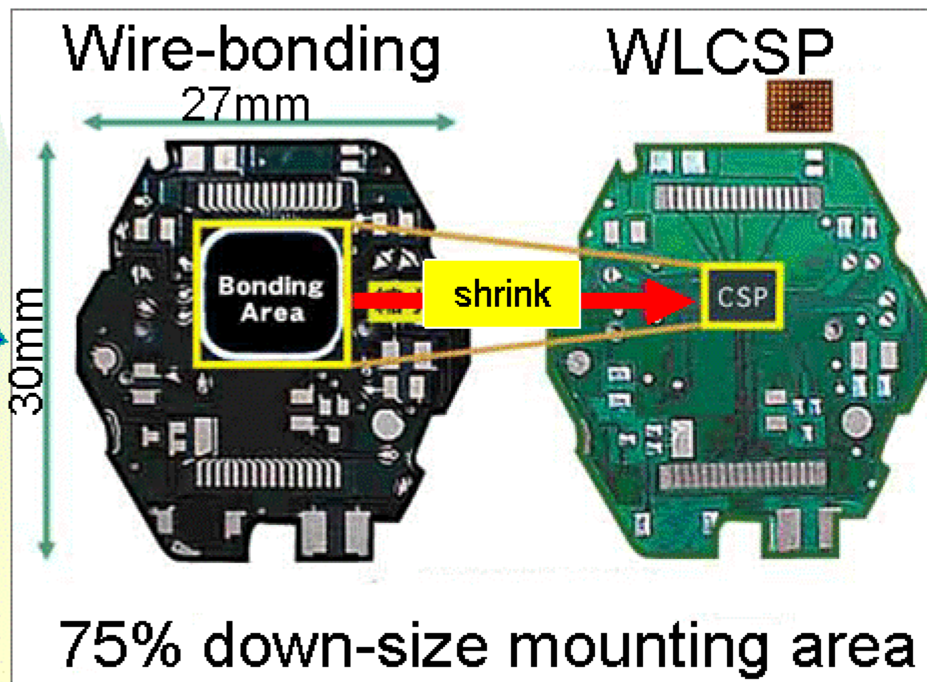


from Future Fab website

Example of WLCSP solution

- Wrist Camera (Fujitsu)
- G-SHOCK Watch (IEP)





from Fujiwara Website

When FS CE not doable then BS CE

- Solder attaches die to PCB
  - Die stable to handle PCB warpage, etc
    - Strength & thinness of “die” important

- For BS CE, die thinned (100-30μm); standard process
  - Mirror-like surface finish needed for trenching

- Use “crystal bond” to mount die

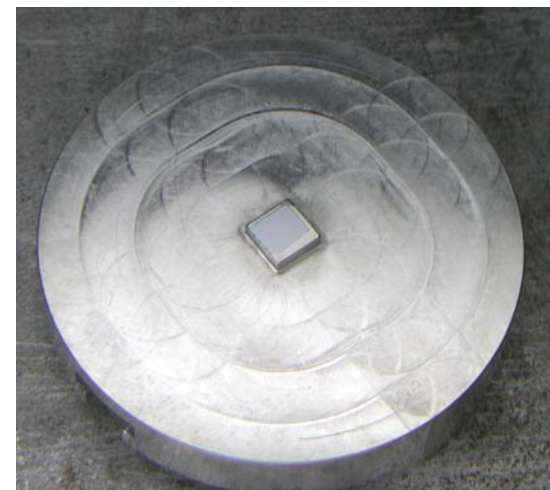
- WL-CSP difficult to handle, not for BS CE **but for post edit functionality**
  - Issue when die to be installed into PCB:
    - **Remove from mount, die “rolls up”**

- **Requirement: Structural strength must be re-established**

Backside Die Thinning

Die sitting on thinning puck ready to be mounted onto puck

Die being mounted with "crystal bond"



Die thinned & ready to be glued onto support

Cloudy surface means not well polished

Re-establish strength of original WL-CSP

- "Glue" silicon plate onto edited die before removing*
  - Gluing must not soften crystal bond temperature (66C)
  - Glue must not dissolve or deteriorate through acetone wash which follows crystal bond removal
  - Glue must be stable through solder process (260C)
- Re-established die dealt with as original
  - Issue: Added silicon to be accurately aligned with original
    - Misalignment limits ultimate placement accuracy
  - "Glue" propsed is Ultra Copper from Permatex
    - Room temperature curing, good for 370C
  - "Glue" proposed is Duralco 132 from Cotronics
    - Room temperature curing, good for 260C

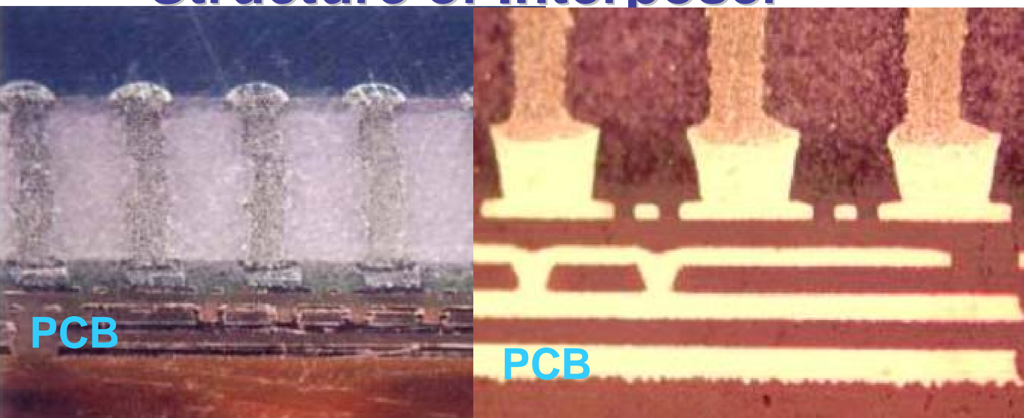
* Si ideal material: no CTE stresses added to thinned die; bonding "glue" must be thin so its CTE can be neglected

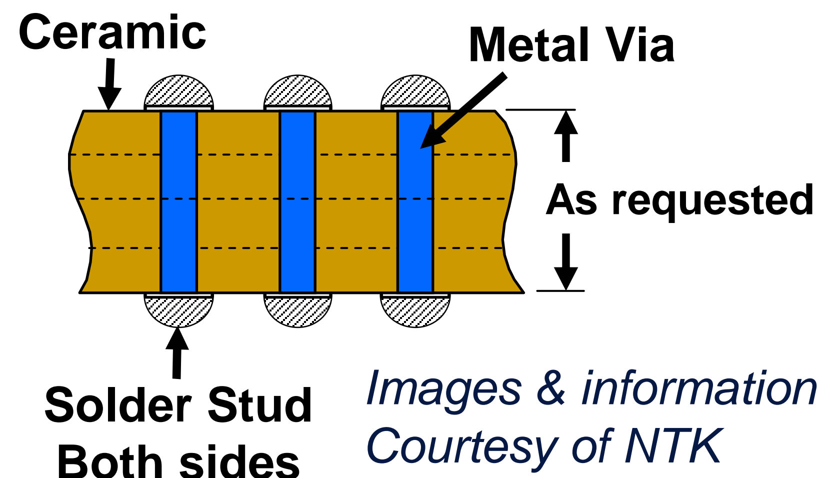
"Socket" as Die Support

- Address curling by gluing die onto PCB-compatible die socket
  - Sacrificed to enable die thinning
- After thinning, die edited & installed onto PCB.
  - Socket is the die support

- PCB-compatible die socket does not exist → interposer
- Die glued onto interposer, thinned & installed onto PCB

- **Structure of Interposer**

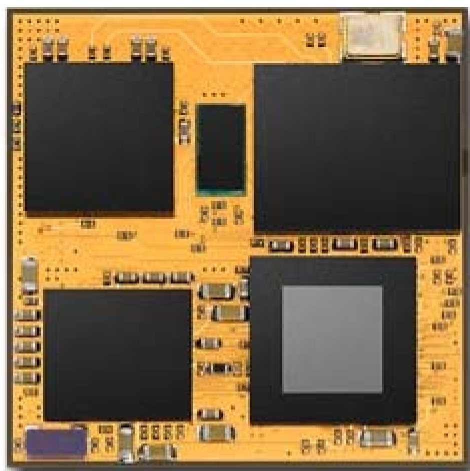




Images & information Courtesy of NTK

PCB as Die Support

- Address curling by installing into **its** PCB
- If die is globally lapped, PCB components removed
- If die of interest milled, all components can remain
- Purpose of CE to test proposed mask change
  and to supply functionality for system level debug

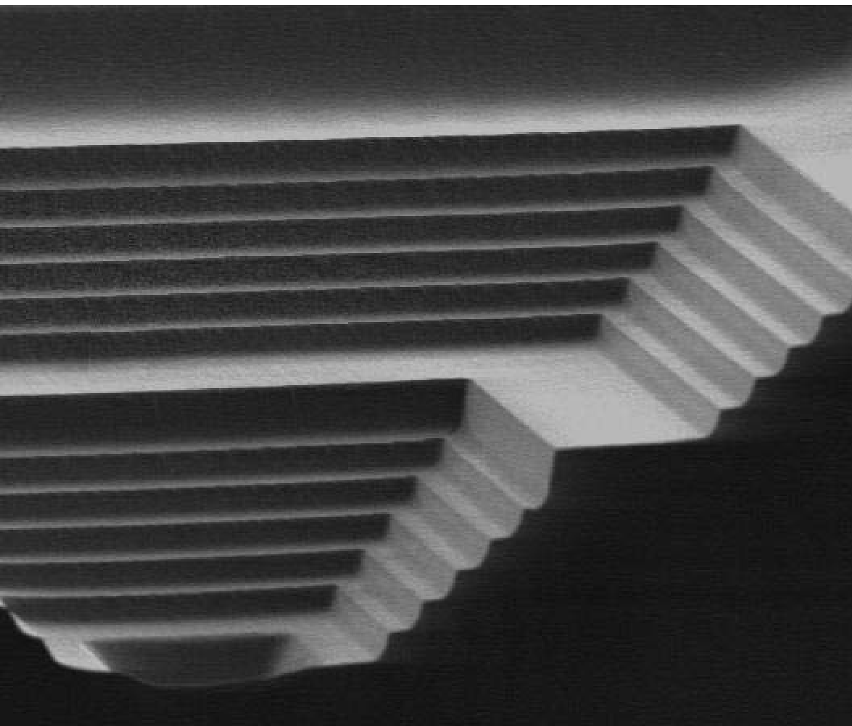


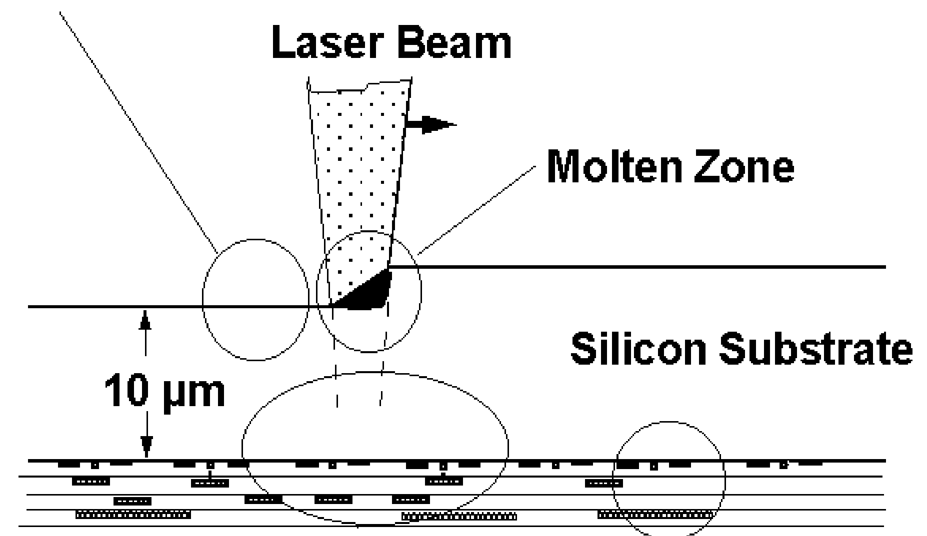
American coin ~size of 1Euro

from Freescale website

Laser Chemical Etching instead of Global Thinning

- Thin die by opening a trench but leaving Si edge sufficiently strong
- Issue: Small die & so much heat→ special fixture needed for thermal dissipation & chemistry protection





from Revise, 1999

Summary

- CE of WL-CSP required
- Key to BS-CE of WL-CSP:

Establish structural strength

- Several ways suggested:
  - Thin & edit on PCB
  - Locally thin with LCE then edit
  - Glue to interposer then thin & edit
  - Thin & edit then glue to new piece of Si
- Most universal approach seems to be interposer

Acknowledgements

- Chun-Cheng Tsao Credence
- Didier Renard Credence
- Frank Tsao AMER
- Jack Vermeulen Ted Pella
- Jeff Large TI
- Jim Colvin FA Instruments
- Mariel Stoops NTK
- Rajesh Jain Credence
- Scott Silverman Varioscale
- Susan Li Spansion
- Tanh Nguyen Credence
- Tim Blade Credence
- Tom Hinton NTK

References

- Jim Colvin, “State of the Art in Backside Sample Prep”, ASM-EDFA AO (2002) 2:5.
- Ravi Chilukuri, David Hays, “Wafer Level Packaging: Yesterday, Today and Tomorrow”, (7/1/2006) Future Fab Intl. Volume 21.
- Susan Li, “Chip Scale Packages and Their Failure Analysis”, ASM-EDFA AO (2003) 1:11.