EUFANET

Full Wafer Level Stacking without TSV
Applications to Memory-only and heterogeneous SiP

Presented by Dr Christian Val
Co-founder and CEO of 3D Plus
408 rue Hélène Boucher
78532 BUC (France)
cval@3d-plus.com

IAS Toulouse Nov. 28th of November
PLAN

- **Introduction**
- Technology of the Stacking of Rebuilt Wafers
- Comparison between PoP/W2W and WDoD
- Applications
- Conclusion
Company Highlights

- Spin off from Thales (1996), from September 2011, 3D Plus is a 100% subsidiary of HEICO company
- Strong R&D from the 3D Plus launching
- Active patenting policy
- Space certifications from CNES, ESA, NASA, JPL, JAXA, CAST etc...
- ISO 9001 from 2003
- Exportation: 90%
- Workforce: 115
- R and D: 12 including 6 PhD
PLAN

- Introduction
- Technology to Stack the Rebuilt Wafers
- Comparison between PoP/W2W and WDoD Technologies
- Applications
- Conclusion
3D Existing Packaging Technology

- Chip-on-Chip
  - Wire bonding
    - Amkor
    - ASE
    - STATS
    - SPIL
    - ...
  - Edge connection
    - Bus metal
    - Bus silver epoxy
    - 3D Plus
    - Irvine Sensors
    - VCI
- Wafer Level Stacking
  - Rebuilt Wafer to Rebuilt wafer
    - Freescale
    - Infineon
    - Etc...
  - Thru-Polymer Via « TPV »
    - 3D Plus
- Wafer to wafer
  - Thru-Si Via « TSV »
    - Samsung
    - IBM
    - INTEL
    - ST Micro
    - Micron
    - Toshiba
    - Etc...
Limits of Wafer to Wafer with TSV

- Non multi sourcing wafers
- Need for smallest possible Via (2µm Ø, leads to a thickness of 20 µm or less → Yield of these filled via is low (redundancy is expected))
- Difficulties with SiP, since die of different sizes
- TSV stresses (keep out zone between 20 to 200 µm)
- Unfortunately impossible to have 100% good wafer → very low global yield
WDoD™ (1) Initial Criteria

- Use of multi sourcing wafers
- Stacking of 10 levels per mm, now
- 20 levels/mm in development
- Size: 100µm around the larger Die
- Stacking of Known Good Rebuilt Wafer (KGRW)
- Possibility to stack Known Good Burn-In Rebuilt Wafer
- Parallel processing/Panelization from A to Z

(1) Wirefree Die on Die – Trade Mark from 3D Plus
FLOW 3  "WDoD"

1 - Carrier lamination

2 - Pick, Flip and place / Die on tape

3 - Compression Molding / Panel encapsulation

4 - Grinding (optional)

5 - De-taping

6 - Redistribution layer "RDL"
History of the development of “Rebuilt Wafers”

- 2002 - WALPACK/3D Plus, ST Micro, CEA/LETI, AXALTO ...
- 2005 – Freescale launched a 200 mm “RCP” Line in Austin (USA)
- 2007 - Freescale launched a 300 mm “RCP” Line in Phoenix (USA)
- 2008 - Infineon launched a 200 mm “eWLB” Line in Dresden (DE)
- 2008 - ASE + STATS ChipPAC launched a 200 mm Line in (Singapur)
- 2009 - ASE launched a 300 mm Line in Singapur (Qualif at the end 2010)
- 2009 - CASIO + CMK has a 200 mm Line in Japan
- 2009 - FUJIKURA launched a 200 mm Line for RF applications in Japan
- 2009 - King Dragon probably launched a 400 mm panel Line in Taiwan
- 2009 - Freescale signed a partnership Agreement with NEPES (Korea) to build a 300 mm Line in Singapur (Qualif at the 3rd quarter of 2010)
- 2010 - NANIUM ex Siemens then Infineon, now Independent Company is qualifying a 300 mm Line in Portugal (Qualif at the 3rd quarter 2010)
- 2010 - Tong Hsing is building a “RCP” Line at the 2nd semester of 2011 in Taiwan

In yellow are the companies which ones we have contacts
FLOW 3 "WDoD"

7 - Gluing on the active side

8 - Stacking of the "Known Good Rebuilt Wafer"

9 - Dicing of the rebuilt and stacked wafers

10 - Dicing street edges plating parallel process (electroless Ni + Au)
FLOW 3  "WDoD"

11 - Laser patterning inside the dicing street edges plated

12 - Electrical test at the wafer level (Before singulation)

13 - Singulation
FLOW 3 "WDoD" with TPV

7 - Taping on the active side

8 - Stacking of the "Known Good Rebuilt Wafer"

9' - Thru - Polymer - Via "TPV"

10' - Plating - "TPV"
FLOW 3  " WDoD" with TPV

11' - Dicing of the rebuilt and stacked wafers

12' - Electrical test at the wafer level
     (Before singulation)

13 - Singulation
PoP and WDoD package
WDoD TV1 Feasibility Test Vehicle (total of 10 dies)

Top side (Bump side)

Back side (Gold)

Solder Bumps

Laser cut
PLAN

- Introduction
- Stacking of Rebuilt Wafers
- Comparison between PoP/W2W and WDoD Technologies
- Applications
- Conclusion
PoP and WDoD package
PLAN

- Introduction
- Stacking of Rebuilt Wafers
- Comparison between PoP/W2W and WDoD Technologies
- Applications
- Conclusion
MEDICAL APPLICATIONS:

- Micro camera for Endoscopy (2,6 x 2,6 mm)
- Modules for Pacemaker, Neuro stimulator
- Module for 40 silicon capacitors on 20 levels
- Earing aids
- X Ray camera with Philips/ Germany
- European program/ e-CUBES with pacemaker
- European program/ e-BRAINS with MEMS

INDUSTRIAL APPLICATIONS

“Structural Health Monitoring”

- Abandoned Sensors for avionics
- Stacking of FPGA (bare die) + DDR3 + PROM for military and industrial applications

NICHE APPLICATIONS
Going further than flip-chip – 3D SiP integration for hearing aids

- Through Silicon Vias (TSV)
- Edge Vertical Routing (Based on 3DPlus technology)
Application WDoD with MEMS – Opposite Twin Cavities Technology for MEMS (Zero Stress, Full Hermeticity)
Structural Health Monitoring
Abandoned Sensors

Diagram at time T

Interrogating Unit
programming and download

cable

vibrating platform
Aero Demonstrator Partnership
workflow – e-CUBES Program

Very complex problem for 100s sensors
To be checked by simulations

3D+

Existing components + energy scavenger

IZM

dies

TAS

U. Paderborn

Innovation proof of concept OK
Demonstration for Y3

TBC

Philips

RTOS

Specs

IMEC

Delay lines

EPFL

Flexfoil

chipset

WUB

Tyndall

Innovation proof of concept OK
Demonstration for Y3

TBC
3D PLUS Demonstrator
e-CUBES Program

- 3D PLUS Module
- Acceleration X
- Acceleration Y
- Acceleration Z
- Temperature
- RH factor
- Pressure
- Switching block
- Events storage memory
- Ultra low power microcontroller
- Smart clock (autonomous and synchronisable)
- Wake-up block
- Wireless interface
- Power Management block
- Micro-battery
- Vibrations energy scavengers
- Configuration and program upload
- Data download
- Vibrations and shocks
Abandoned Sensors e-CUBES Program

- 1 RH and 1 P transducers on top
- 1 T transducer on each face
- Pads on bottom for connexions to the RF block
- Pads at the top (energy + “rescue operations”)
- Specific anti-screwing fixation
- Internal cube = 8 mm X 8 mm X 14 mm (Target: 6 x 6 x 6 mm/ 0.22 cm^3)
VOLUME APPLICATIONS

- **SRAM Modules**
  - 8 memories (1mm with balling)

- **Mega SIM**
  - 5 levels within 500 µm (in a cavity inside the standard 800 µm SIM Card)

- **DDR3 stacking for wide Bus** (in process with Nanium ex Siemens/Infineon in Europe)
MEGA SIM

- 4 Flash
- 1 Microcontroller
- Silicon Capacitors
- Oscillator
- 8 ISO Contacts on top

To be embedded in card or key
WDoD™ Status

- Proof of Concept – completed (2002-2005)
  - European funding (25 M$) with CEA/LETI, AXALTO, ST Microelectronics, 3D PLUS, …

- Process Development & Optimization of WDoD (from 2006 up to Feb 2009) with NXP/Philips semiconductor

- From Feb 2009 Prototyping with the RCP Process from Freescale/Phoenix

- Functional Prototypes with Nanium. Stack of 4 DDR3/JEDEC Qualification (end of 2011)
PLAN

- Introduction
- Stacking of Rebuilt Wafers
- Comparison between PoP/W2W and WDoD Technologies
- Applications
- Conclusion
Conclusion and perspectives

- Miniaturization for Consumer, Medical and security domains demands very high interconnection densities and low costs. Reconsidering former experiences: Hybrids, Multichip Modules, Wafer Scale Integration (20 years ago), PoP instead of PiP; we learned that the yield constituted an important part of the production costs.

- The WDoD process only allows to stack Known Good Rebuilt Wafers.

- Several applications in the medical and industrial and large volume areas have been presented.

- This important densification of 10, soon 20 levels per mm, allows to launch extremely ambitious applications in the field of System in Package for Memory-only and SiP for Smart cards and Mobile phone.
Ultra Dense 3-D Micro System with WDoD
Thank you for your attention

www.3d-plus.com